NeoSilicon based nanoelectromechanical information devices

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Collaboration

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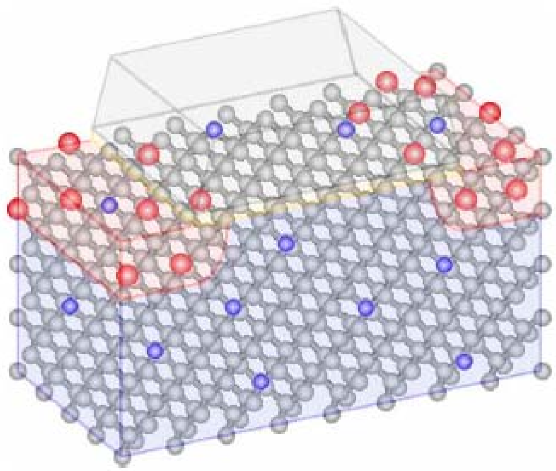
Tokyo Univ. A & T: N. Koshida
Tokyo Institute of Technology: K. Uchida, T. Kodera, T. Ishikawa, T. Nagami, G. Yamahata, J Ogi

Funding

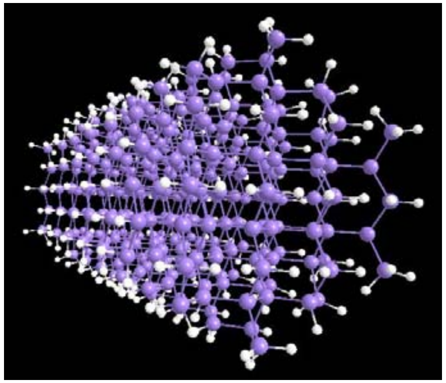
JST-CREST, SORST
JSPS-Kakenhi

Top-down & bottom-up Si nanoelectronics

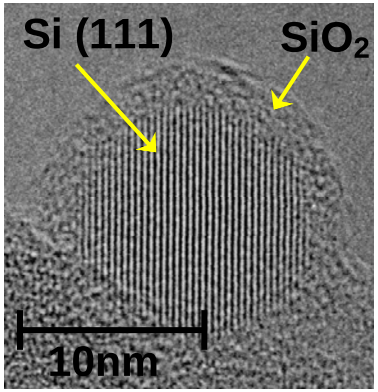


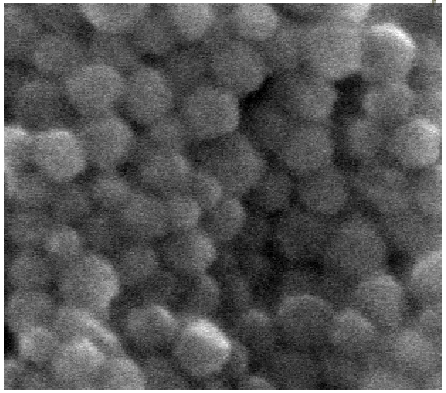
Structures of less than 10nm with short intervals are difficult to prepare by top-down technology.

TOP-DOWN SILICON

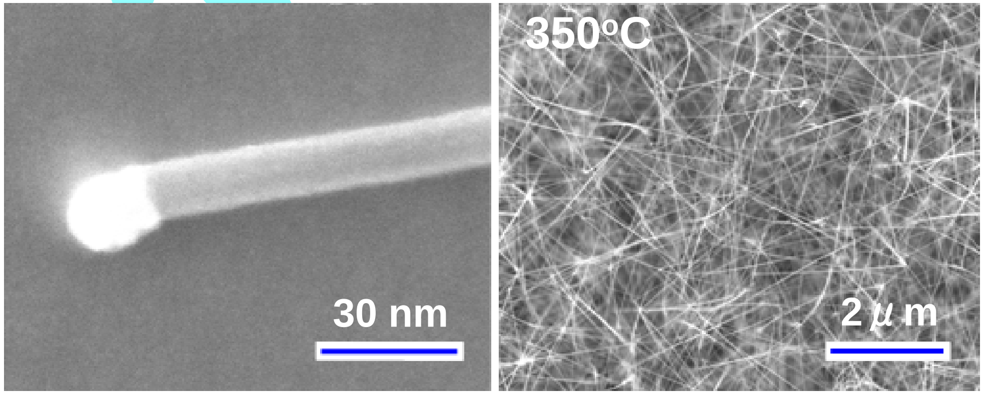


BOTTOM-UP SILICON





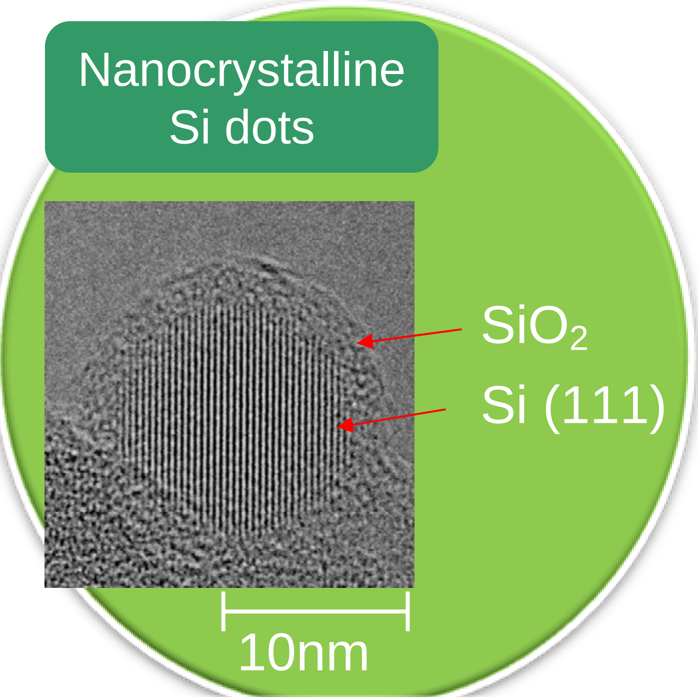
Si nanodots

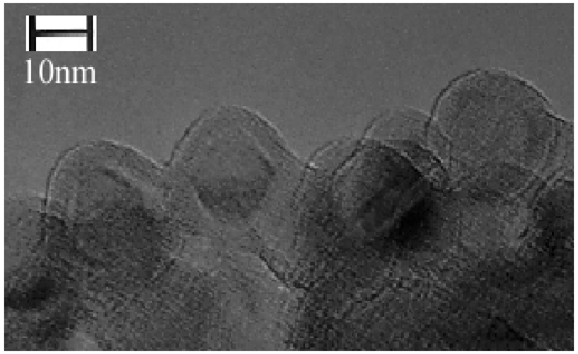


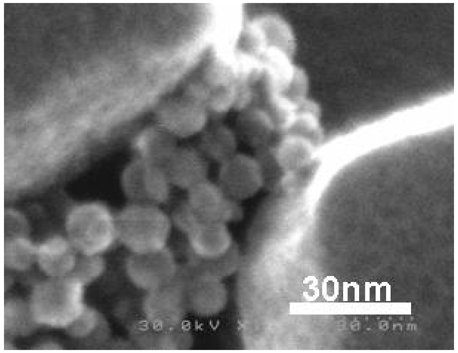
Si nanowires

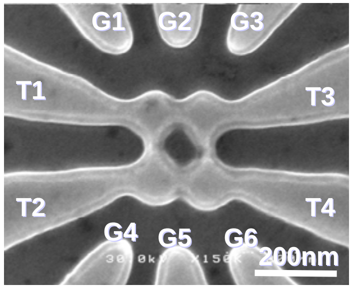
NeoSilicon

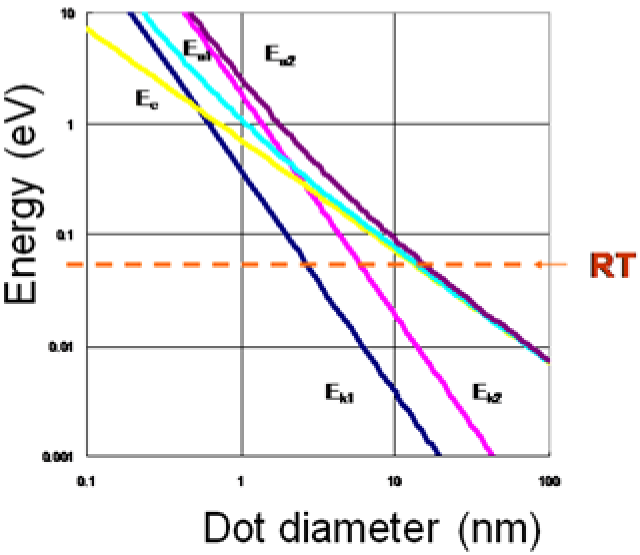
Si quantum dots with the diameter < 10 nm and strong interdot interactions





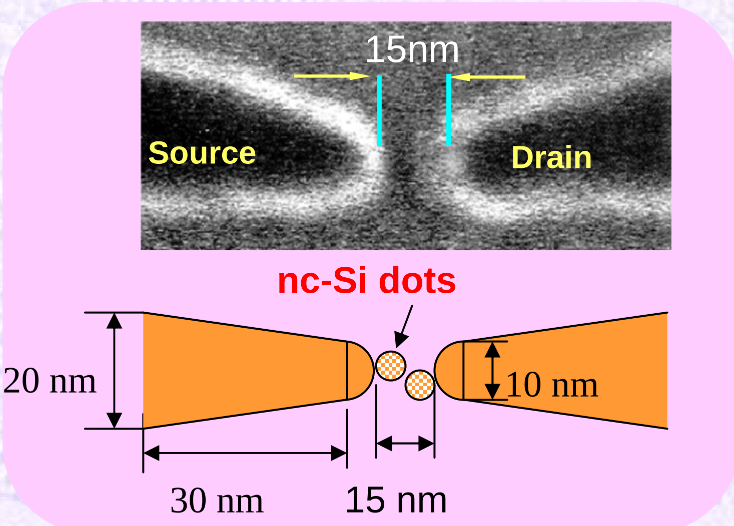


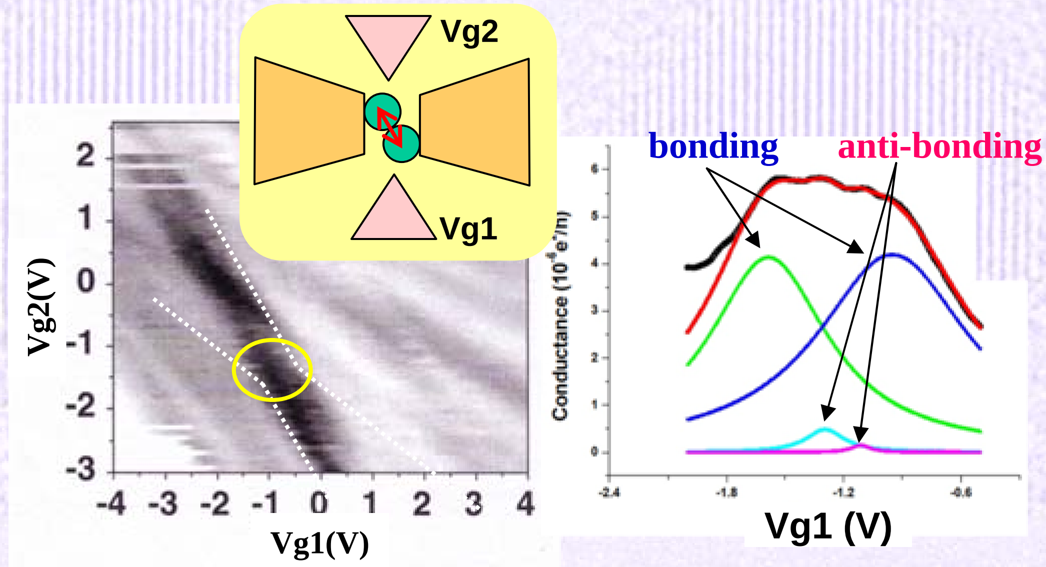




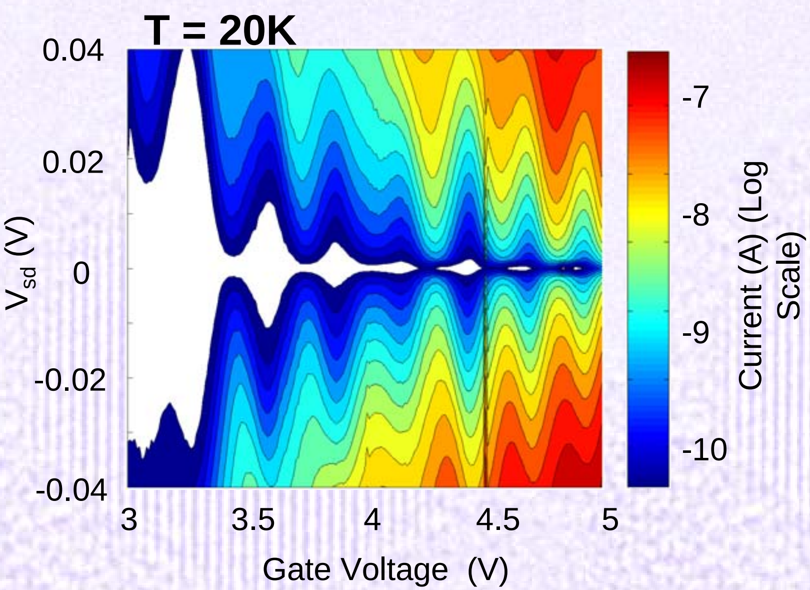
- Bandgaps are determined by nanocrystal size due to quantum effects.
- Conductivity is determined by tunneling.
- High-efficiency light emission
- High-efficiency electron emission
- Coupled quantum dots create new functions

Unique transport phenomena

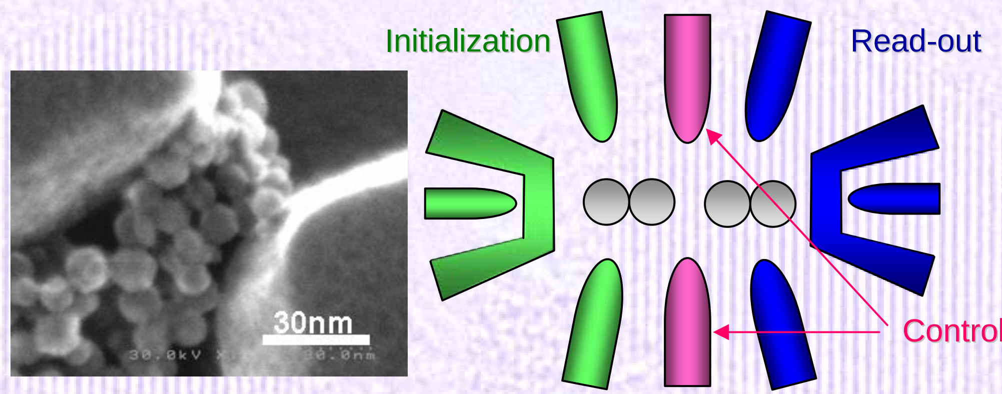




Quantum mechanical interactions in adjacent dots

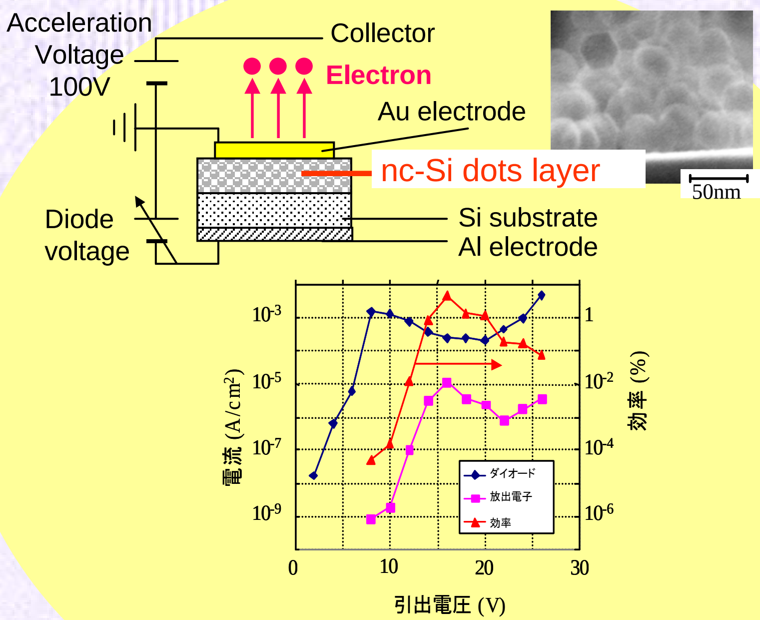


Single-electron tunneling

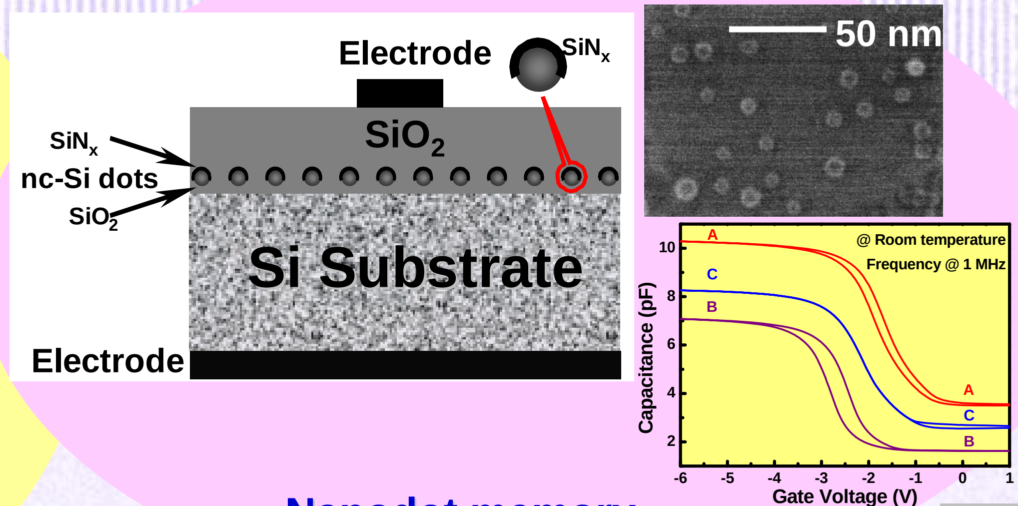


Design & fabrication of nc-Si quantum information devices for solid-state quantum computers

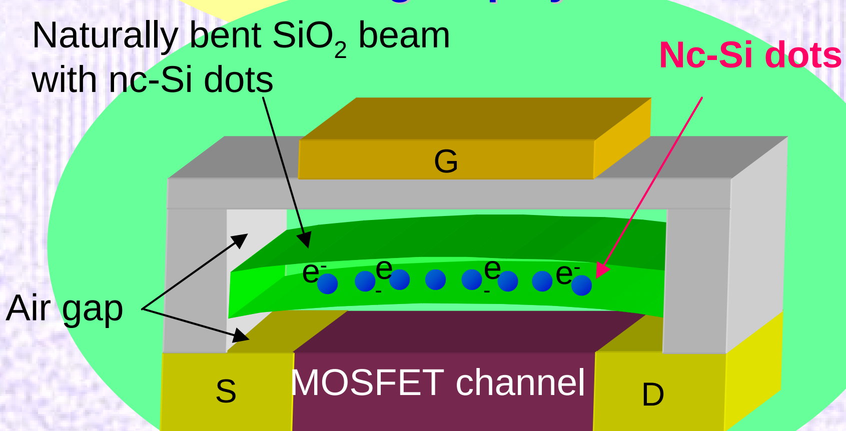
A variety of new applications



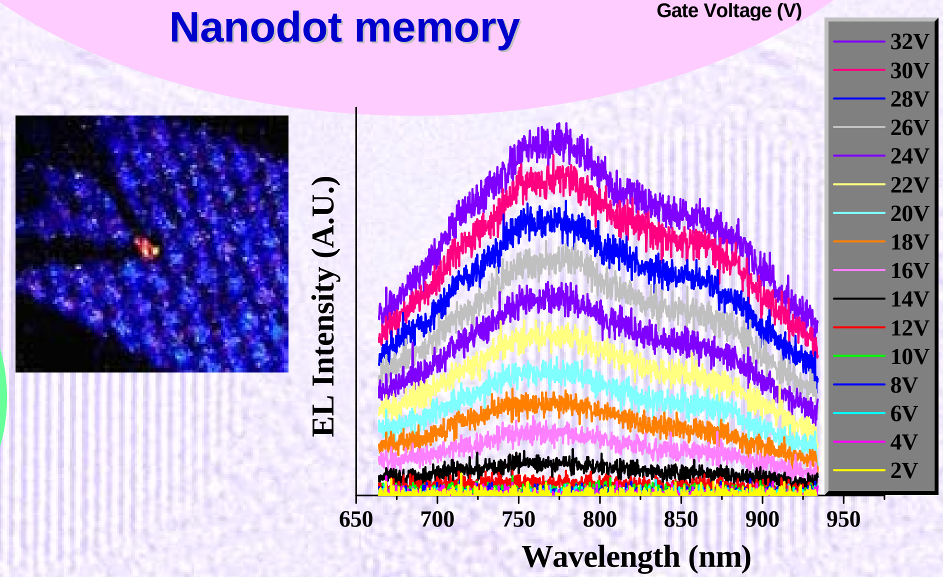
Ballistic electron surface emitting display



Nanodot memory



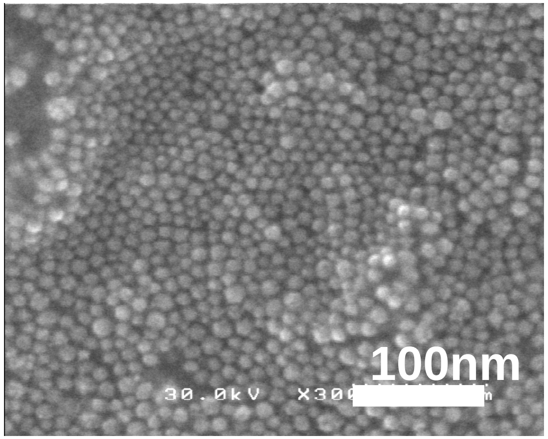
Nanoelectromechanical devices

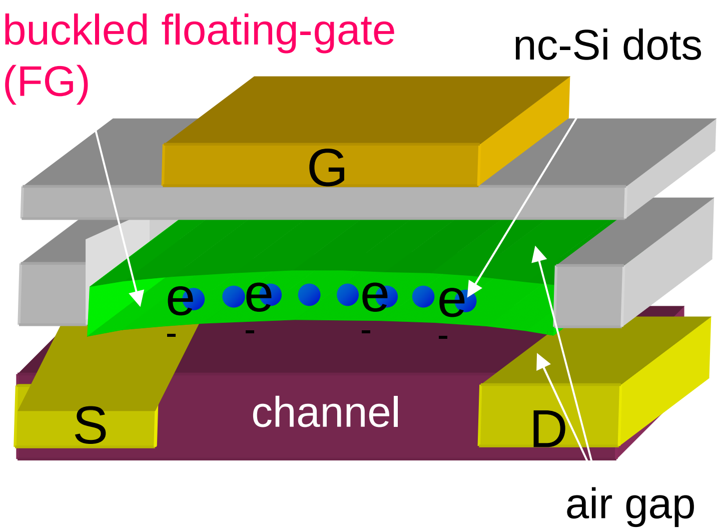


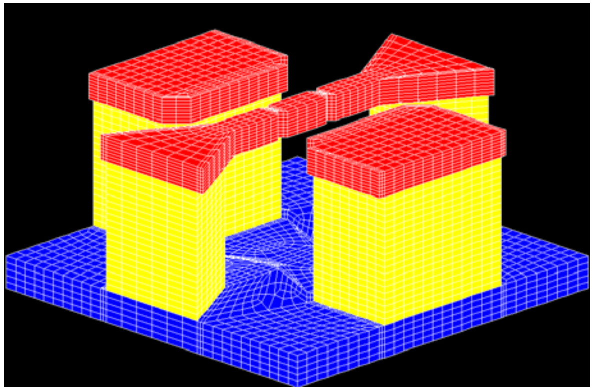
Light-emitting devices

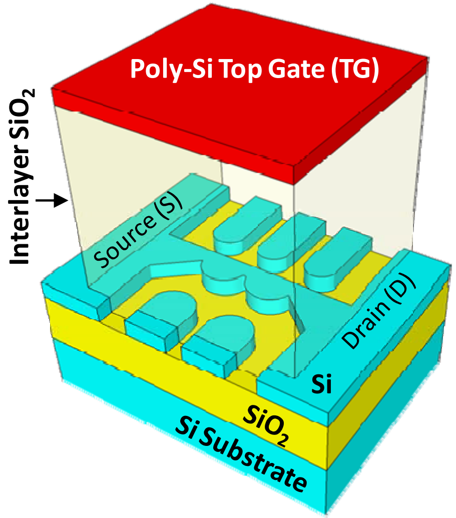
Outline

- **Dot Assembly** T. Ishikawa, Y. Nakamine
- **NEMS Memory** T. Nagami
- **Nano-bridge Transistors** J. Ogi
- **Coupled Quantum Dots** G. Yamahata

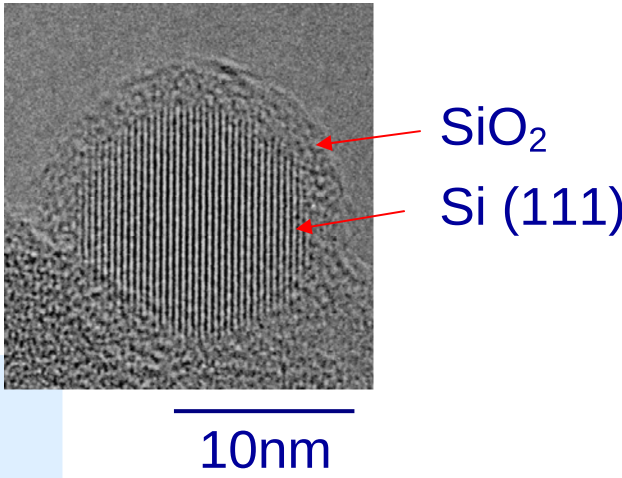




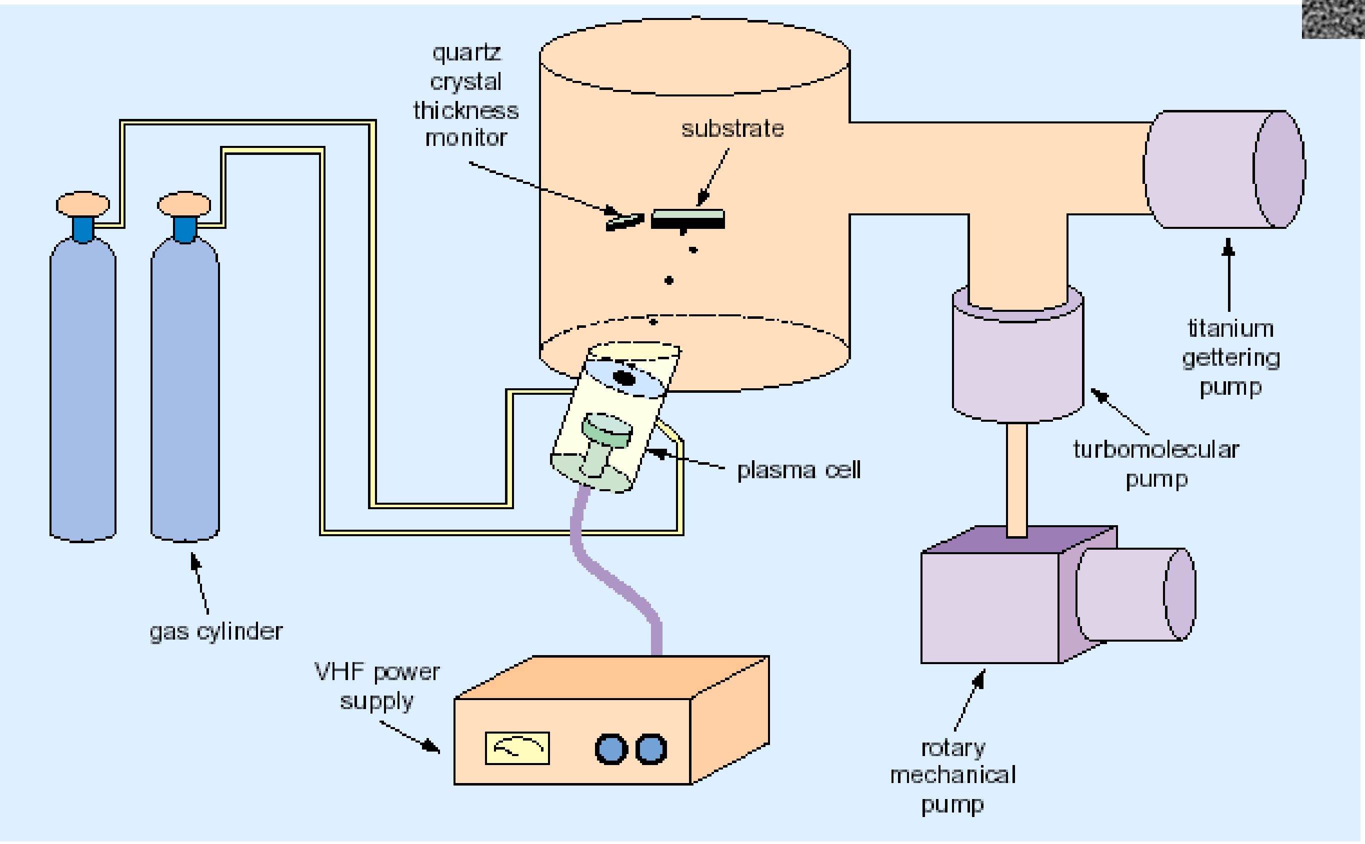




Fabrication of Nanocrystalline Si



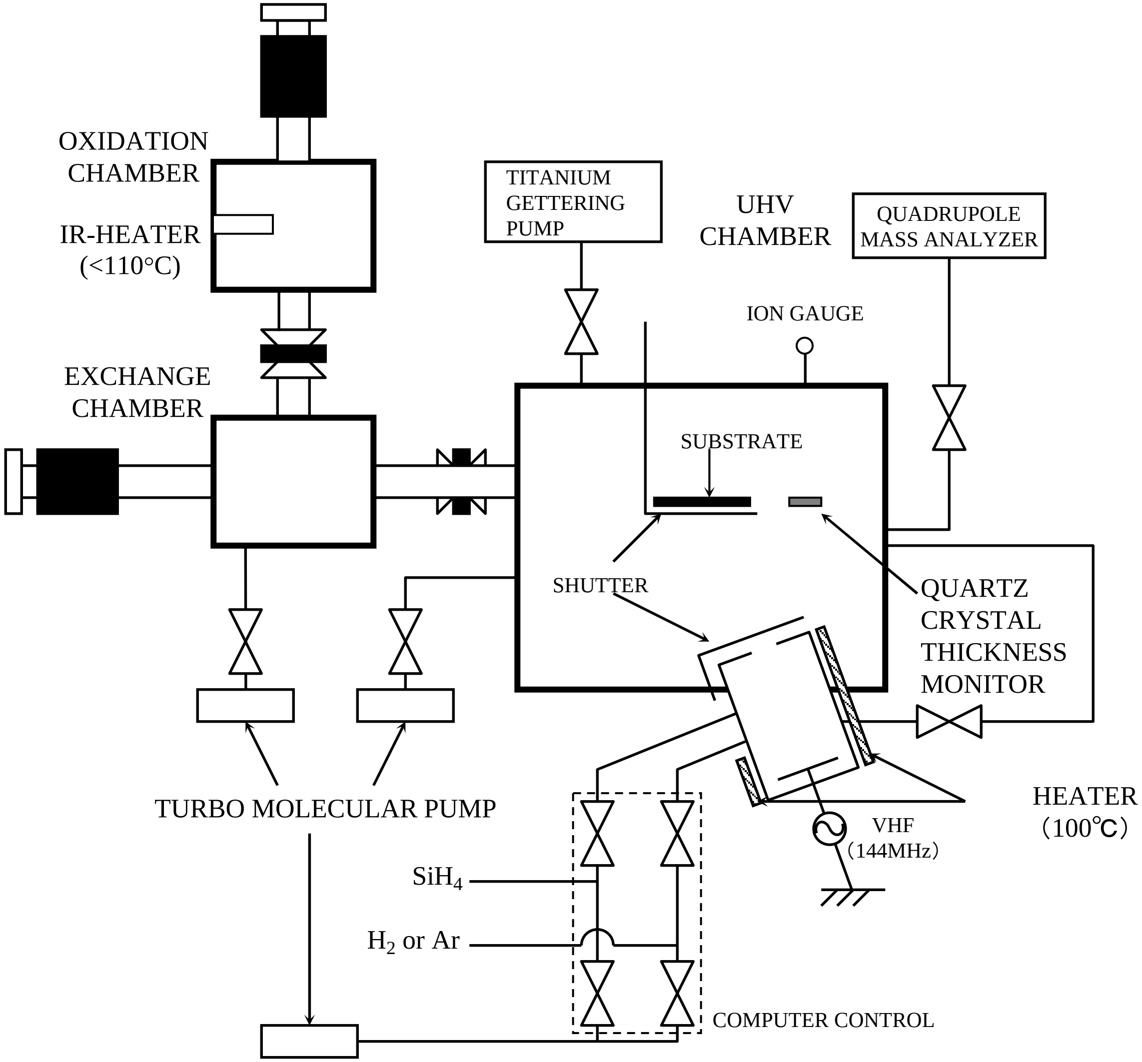
Si Quantum dots formed in VHF Plasma Cell
Low-Temperature Processes



Spherical Single crystal covered by natural oxide.

Single electron devices, high efficiency PL, electron emission.

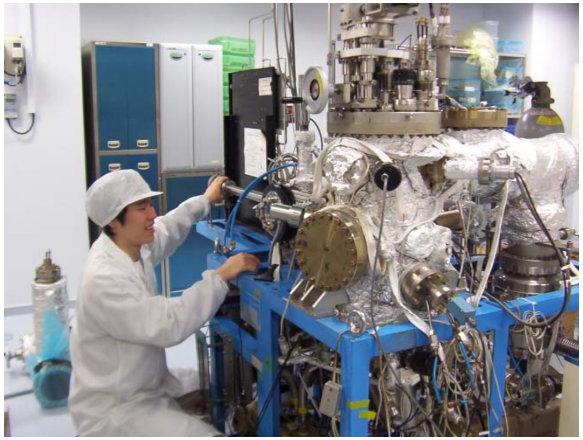
Fabrication of Nanocrystalline Si

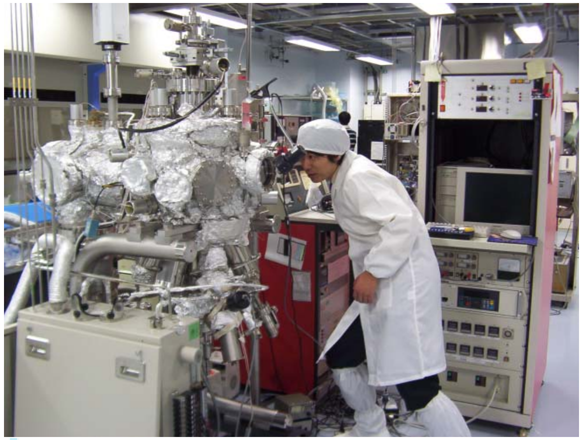


Low-temperature crystal growth.

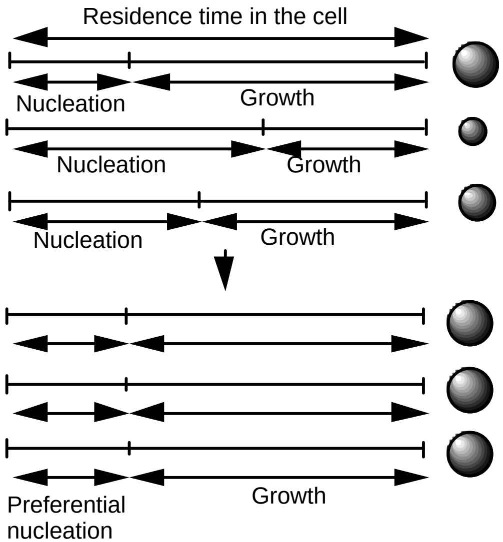
Plasma cell at 100°C.

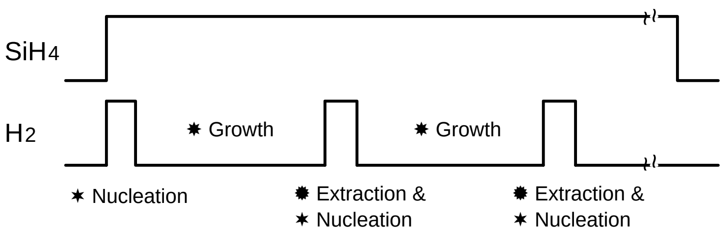
Substrate unheated.

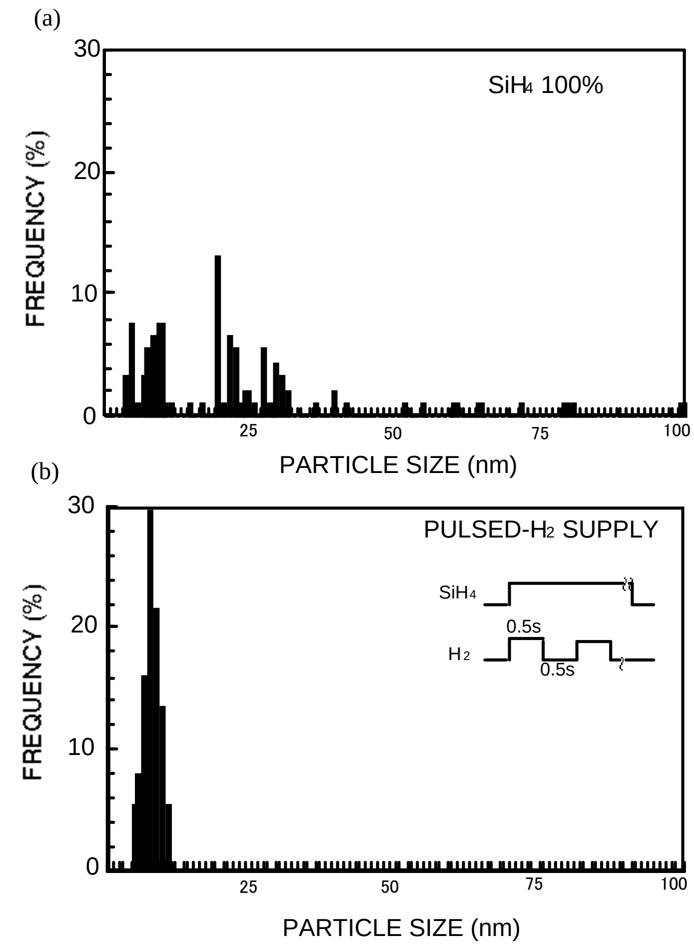




Silicon Nanocrystal Deposition: Size Control







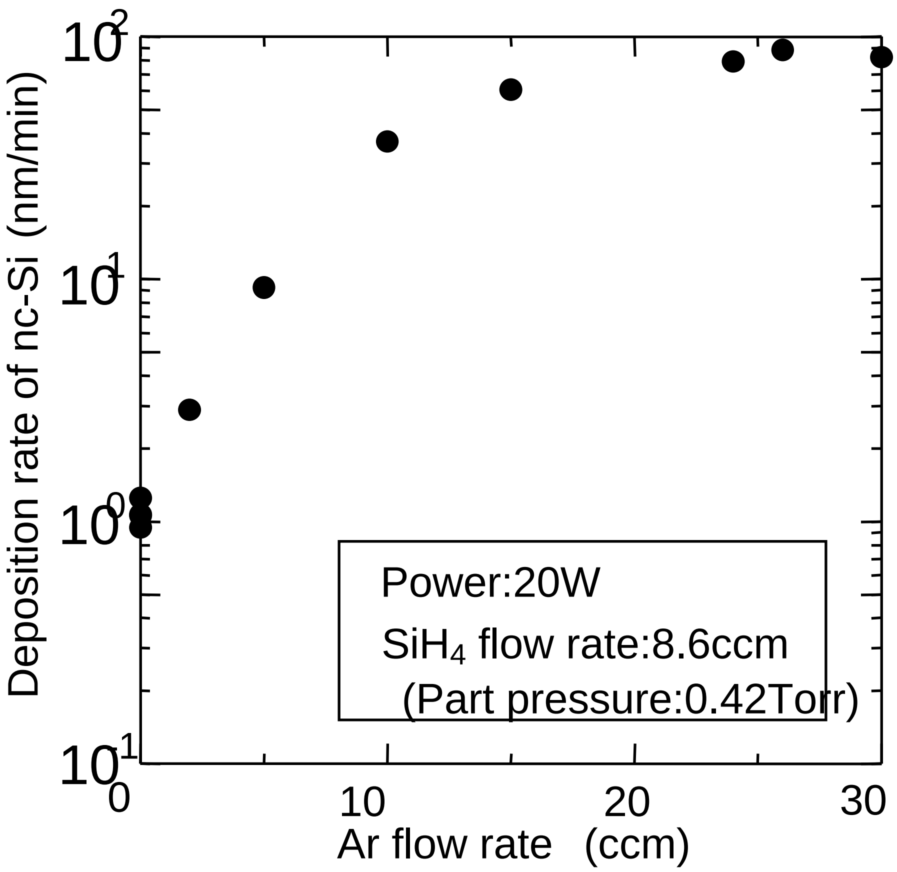
Point: Separation of nucleation and growth

Silicon nanocrystals of 8±1nm.

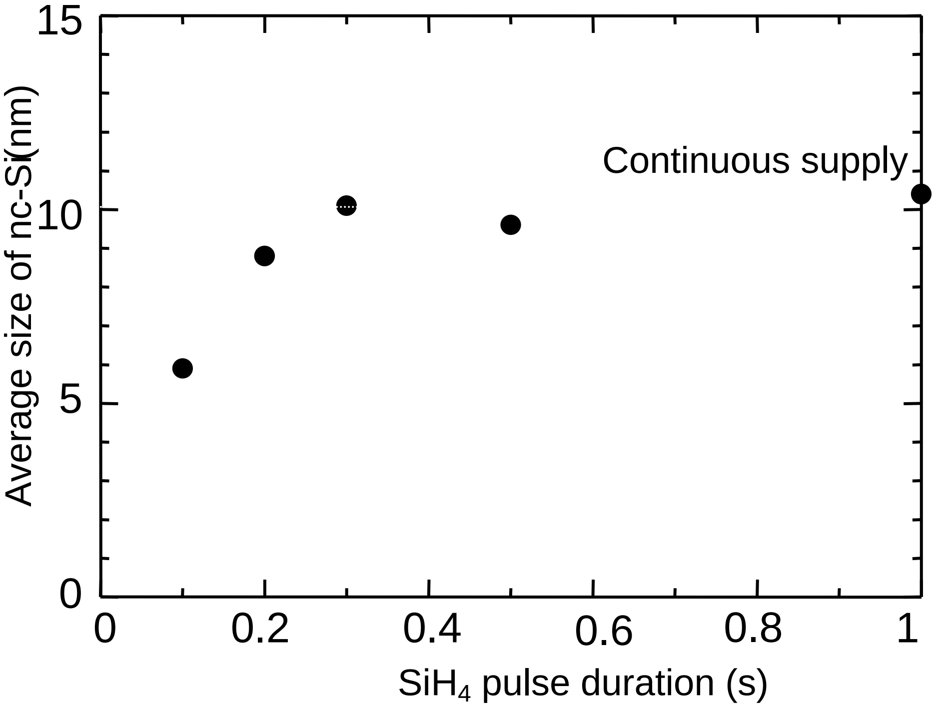
T. Ifuku *et al.*, Jpn. J. Appl. Phys. **36**, 4031 (1997).

Silicon Nanocrystal Deposition: Ar Dilution

Ar dilution enhances deposition rates.

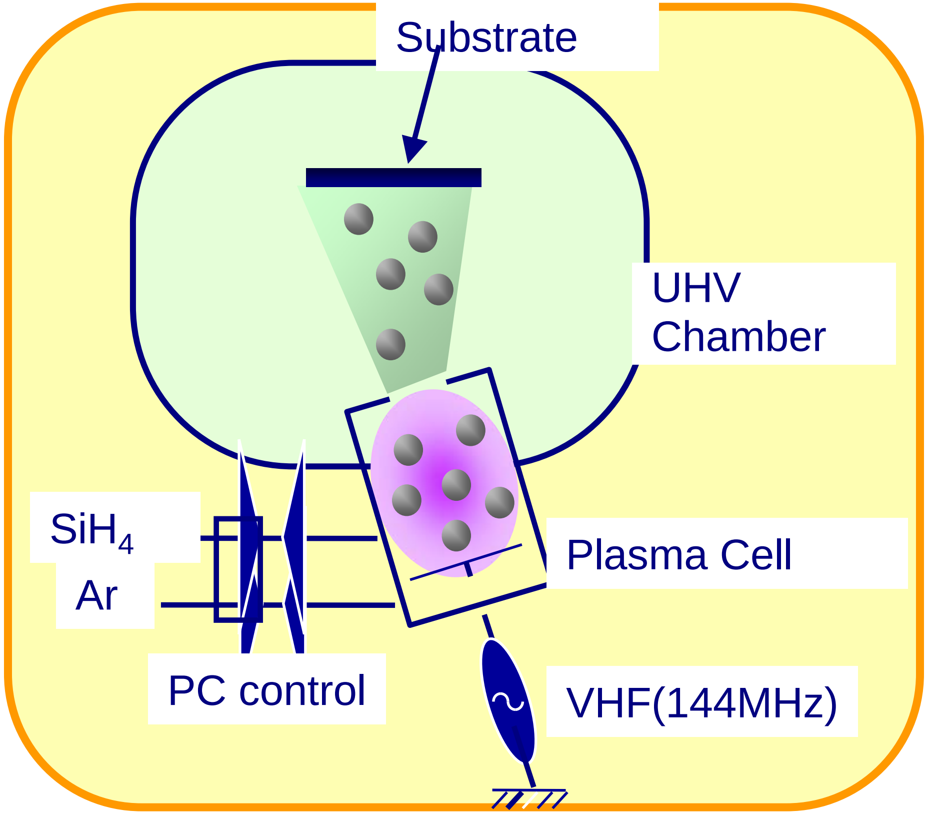


Short SiH_4 pulse results in small dots.

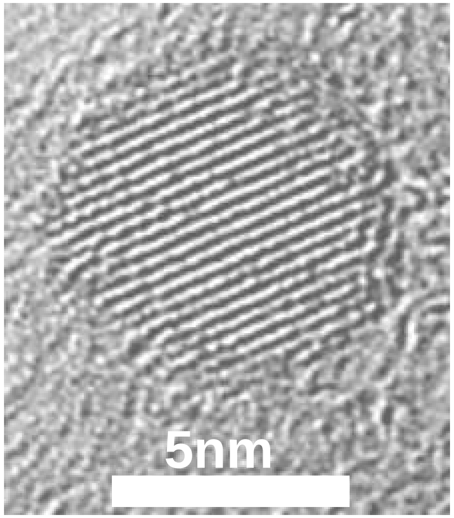


Silicon Nanocrystal Deposition: Ar Dilution

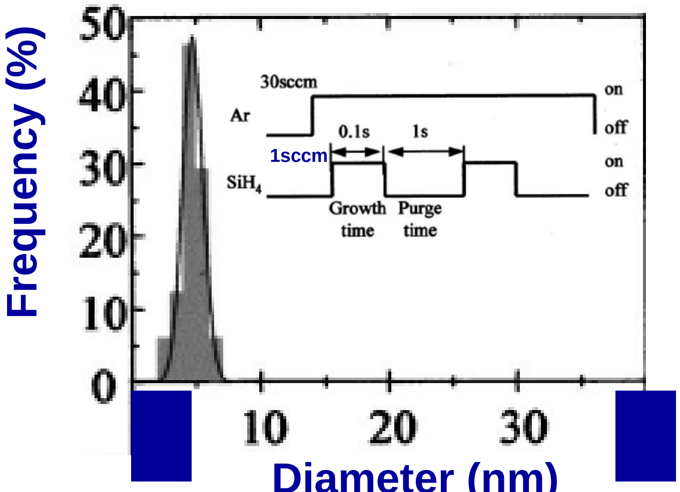
VHF digital plasma process



T. Ifuku *et al.,* Jpn. J. Appl. Phys. **36**, 4031 (1997).
K. Nishiguchi *et al*., J. Appl. Phys. **92**, 2748 (2002)

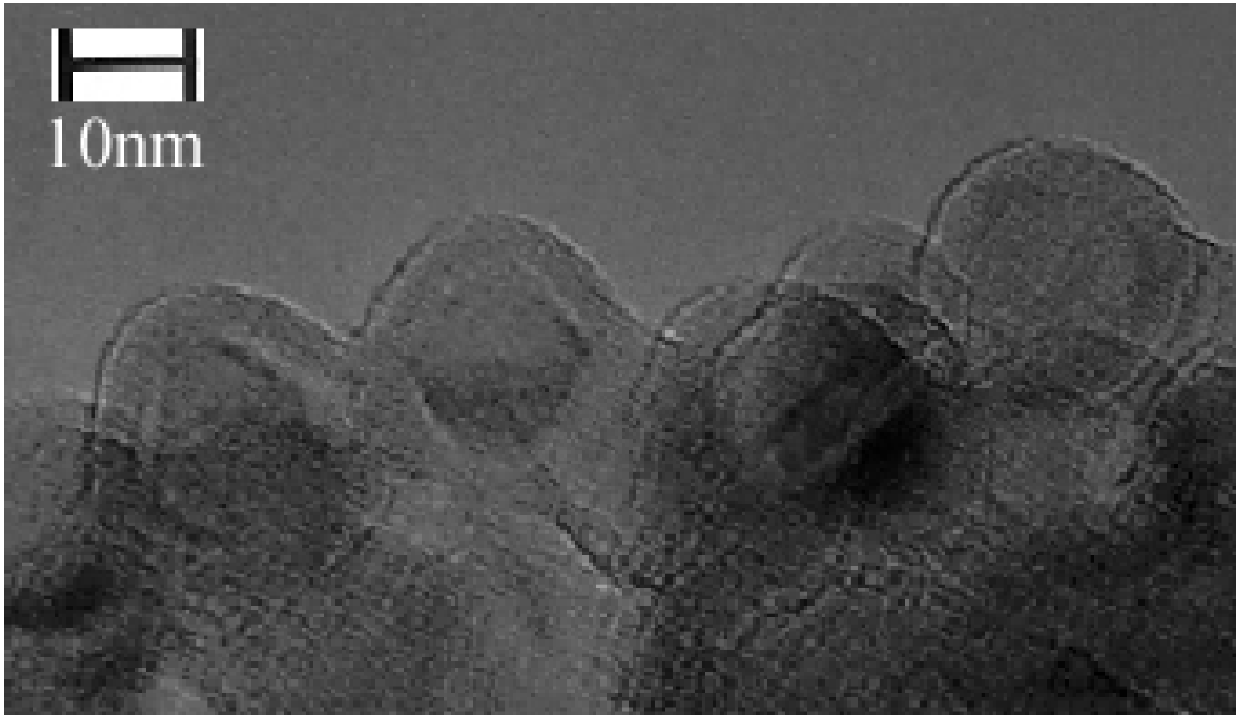


Crystalline SND (d ~ 6 nm)



Small diameter distribution

Silicon Nanocrystal: Surface Control



Surface Properties Control

In *situ Oxidation/ Nitridation*

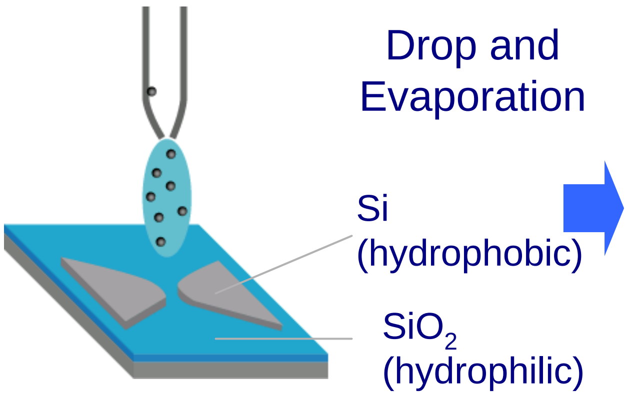
Controlled formation of tunnel barriers and proper passivation of dangling bonds.

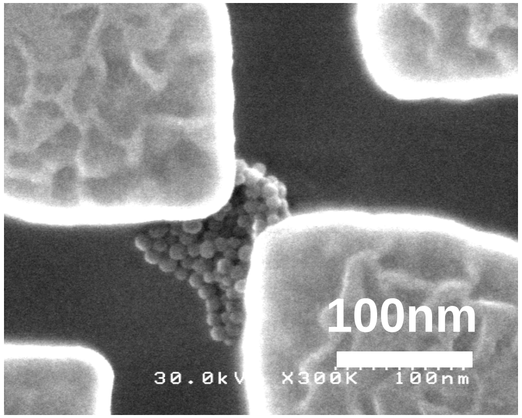
NeoSilicon Fabrication & Integration

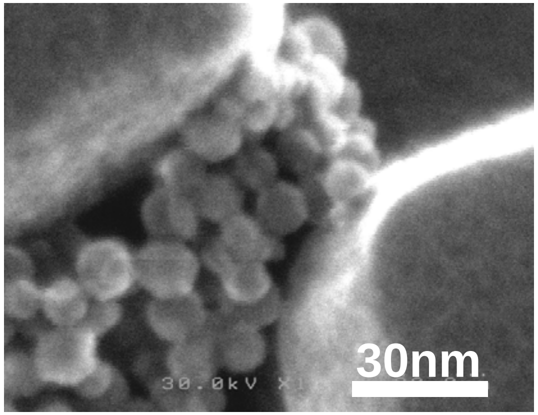
Local area assembly

1. D&E on wettability-controlled substrate

A. Tanaka *et al*., Current Appl. Phys. **6**, 344-347 (2006).

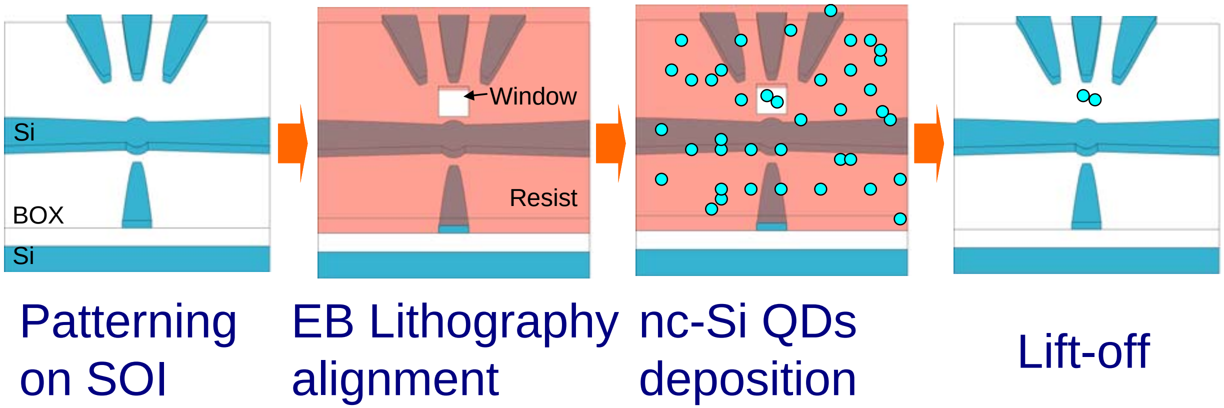


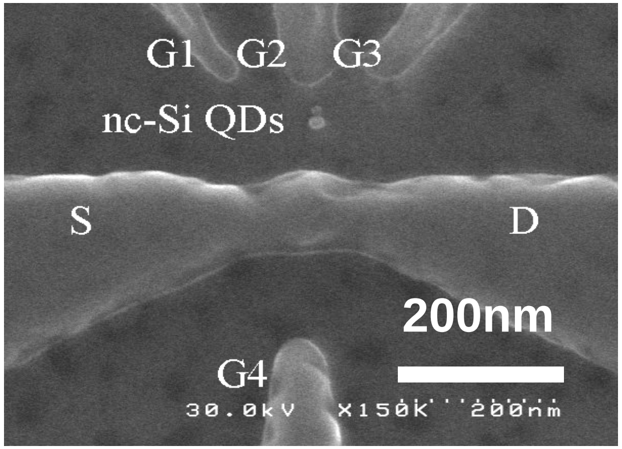




2. Combined with fine alignment technology in EB lithography

Y. Kawata *et al*., Jpn. J. Appl. Phys. **46**, 4386-4389 (2007).



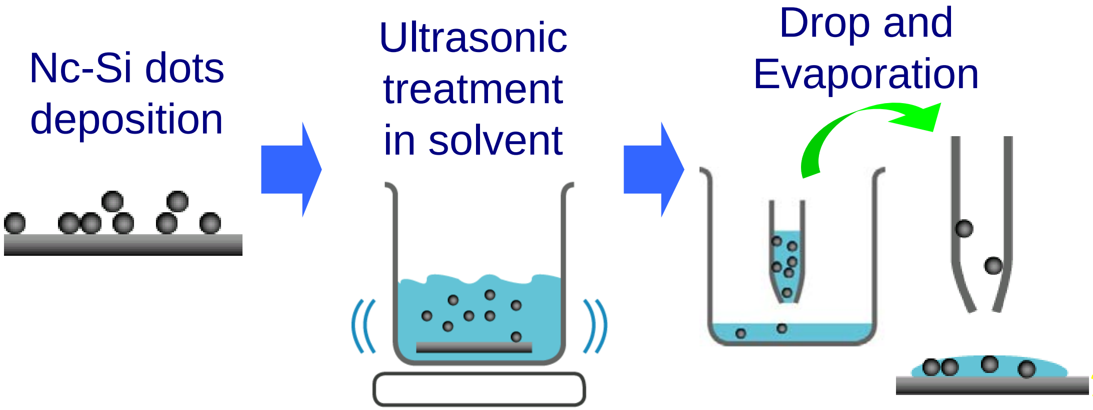


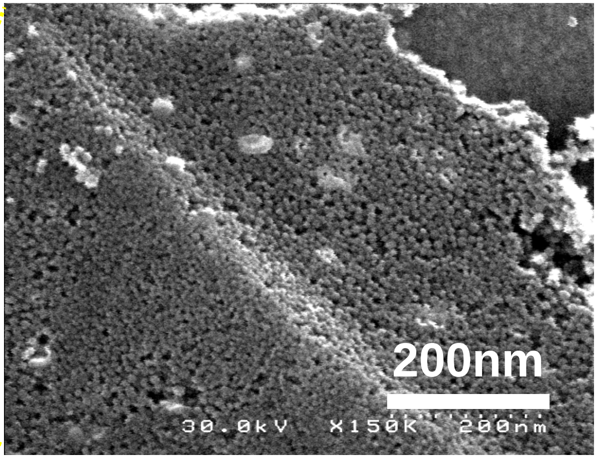
NeoSilicon Fabrication & Integration

Large area assembly

1. SNDs solution →Drop & Evaporation

A. Tanaka *et al*., Current Appl. Phys. **6**, 344-347 (2006).

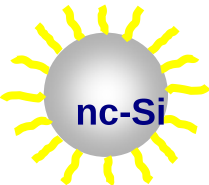




2. Application of Langmuir- Blodgett method to SNDs

A. Tanaka *et al*., AMN-3, Wellington, New Zealand, February 11-16, 2007.

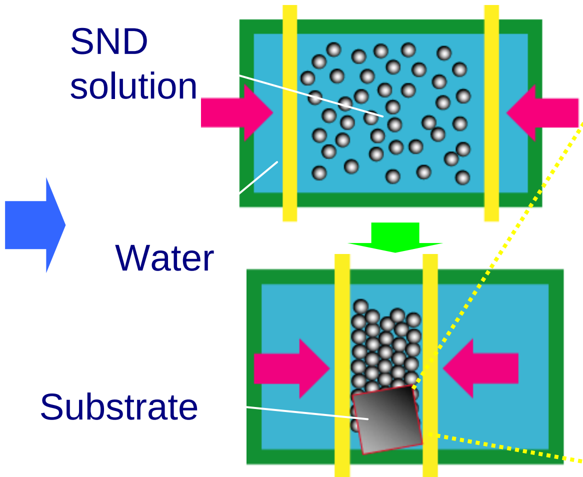
SND surface modification

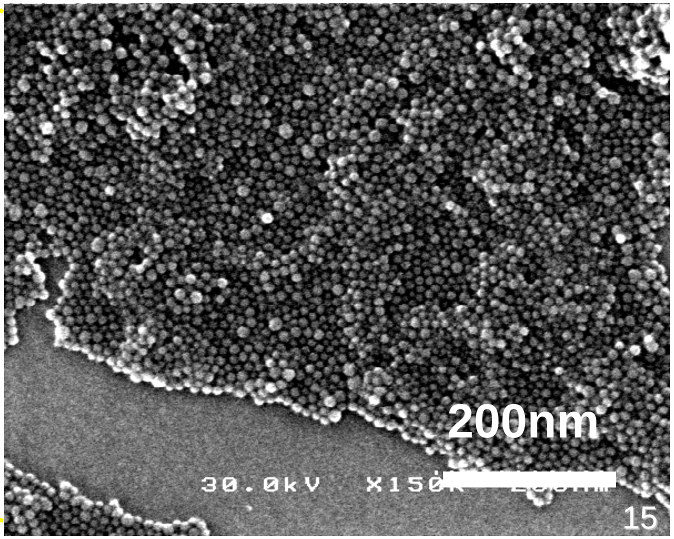


- Protected from water
- Dispersed in hydrophobic sol.

Coated by HMDS
Solvent : $CHCl_3$

LB method

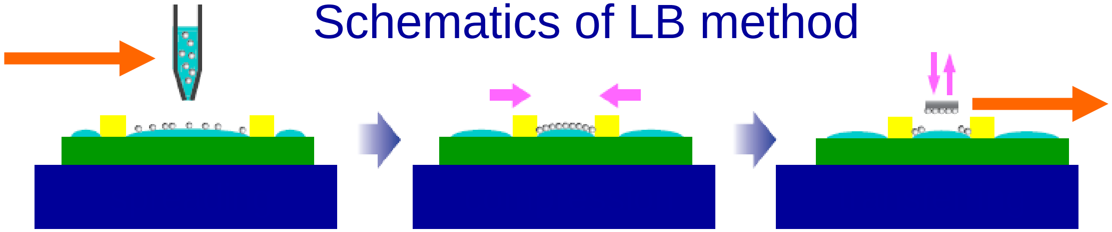




Langmuir-Blodgett method

Dispersed
In chloroform

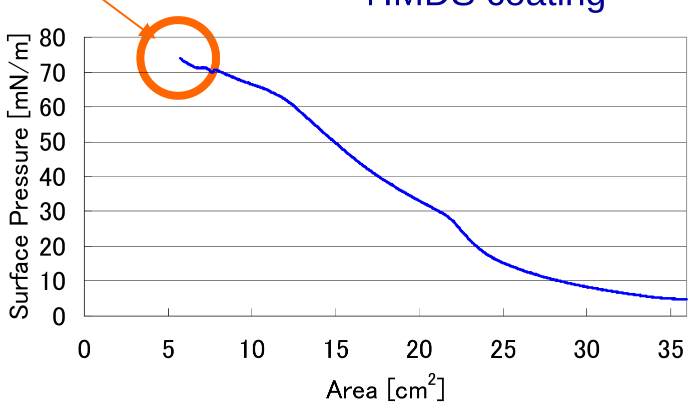
Schematics of LB method

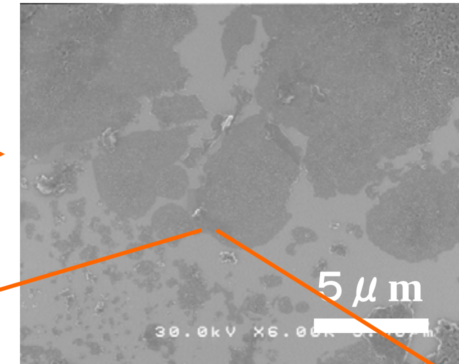


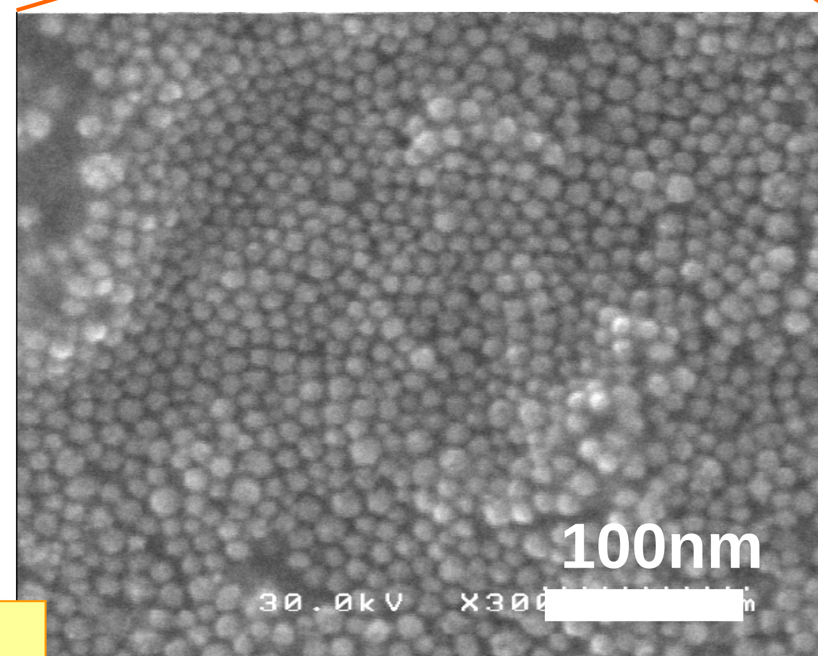
<u>Problems & Solutions</u>

- Hydrophobic and highly-volatile solvent required
  → dispersed in chloroform
- SiND is reacted with water
  → HMDS coating

transferring





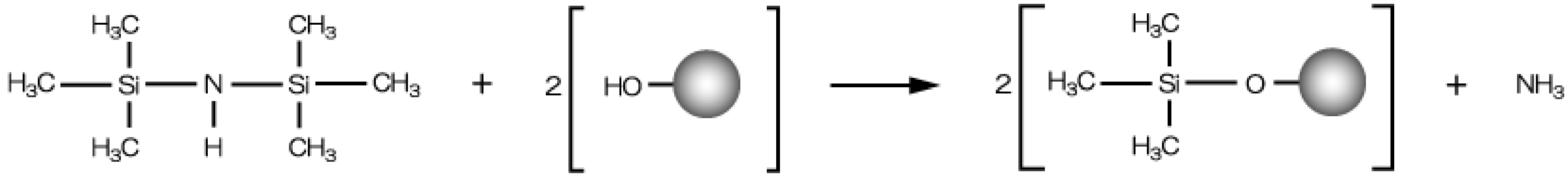


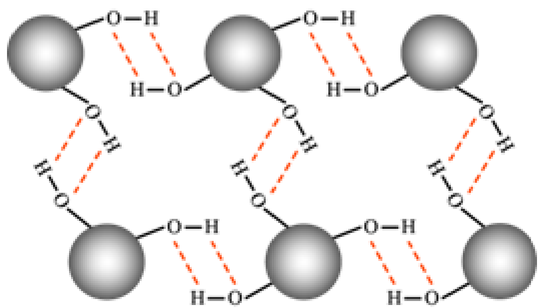
Area density ~ 7.22×10^{11} dots/cm^2

Succeeded in formation of
2D array of surface modified SiND
but not the whole area of the chip

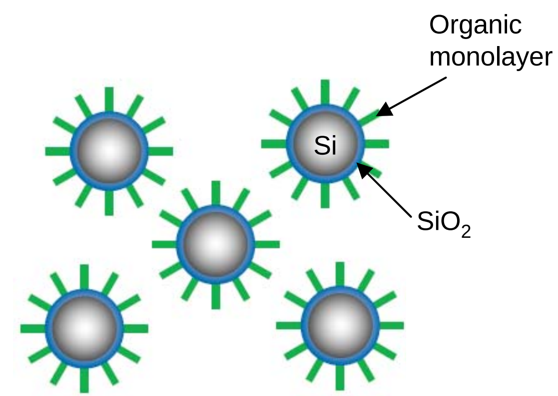
Surface modification of Si nanocrystals

Modification by silane coupling agent (HMDS: Hexamethyldisilazane)





Surface modification



Many nc-Si particles aggregate by hydrogen bonding

→ **Inhomogeneous solution**

Cluster size → large

Decrease of the number of hydrogen bonding

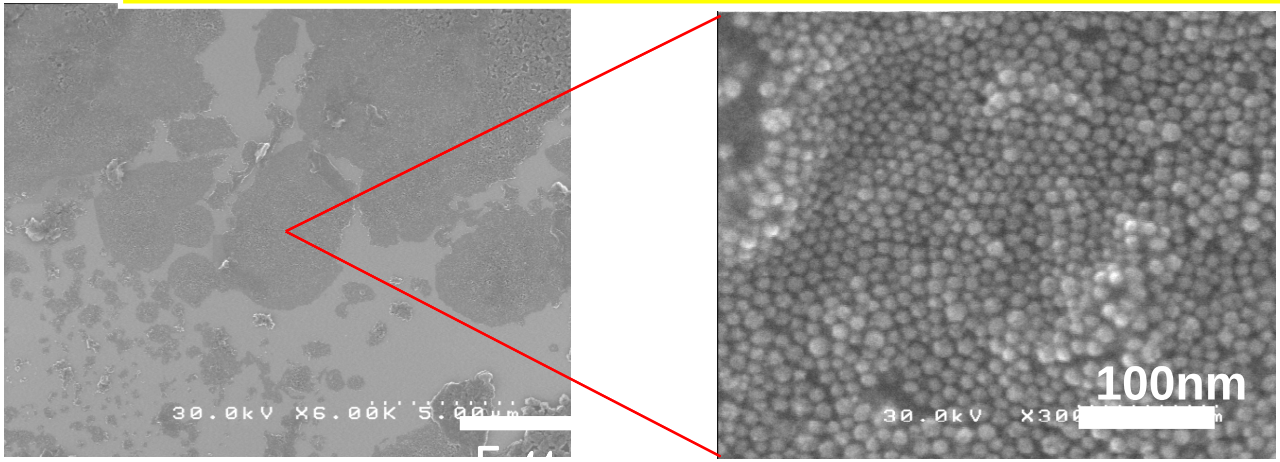
→ **Well dispersed solution**

Cluster size → small

(Ideal size is 10 nm)

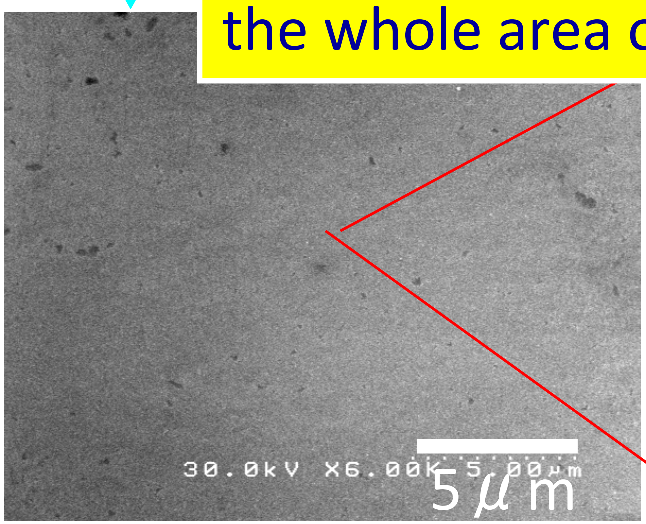
Large area 2D array of SiND by LB method

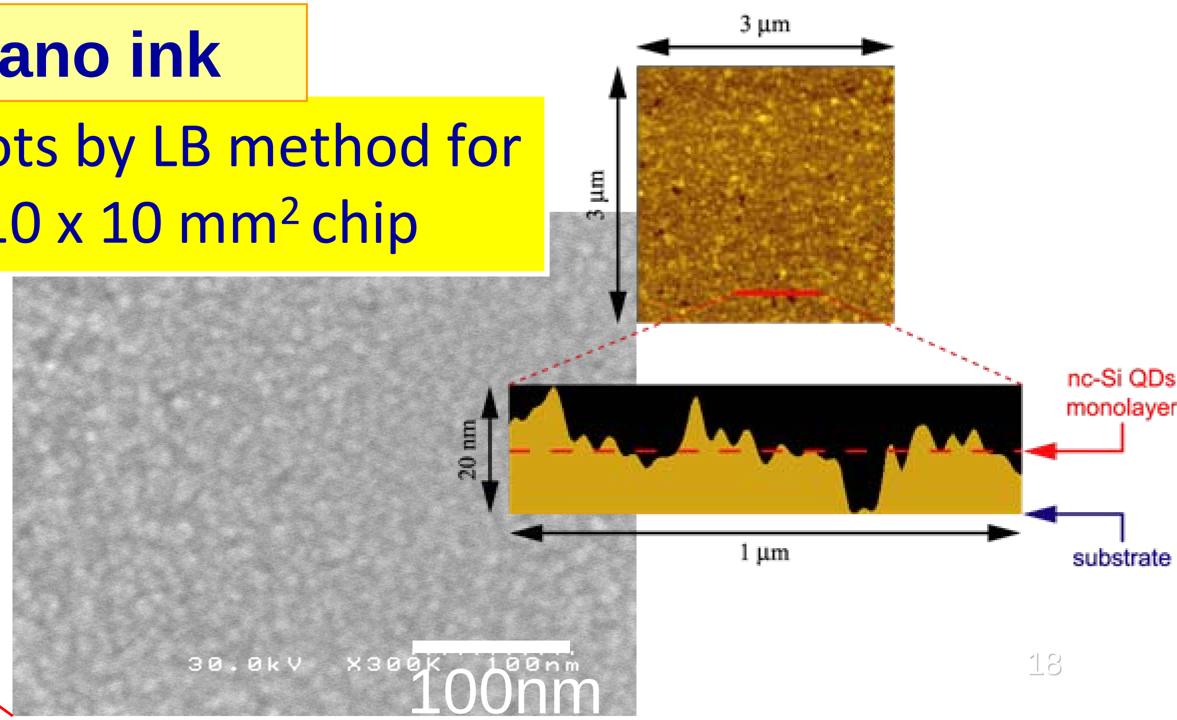
2D array of nc-Si dots by LB method for 5 x 5 μm^2



Optimized Si nano ink

2D array of nc-Si dots by LB method for the whole area of 10 x 10 mm^2 chip

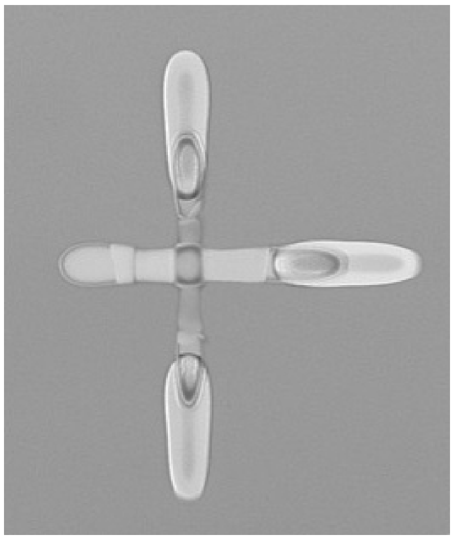




Printable Si quantum dots using nano Si ink

Printed Silicon

Thin-film transistor fabricated by printing technology



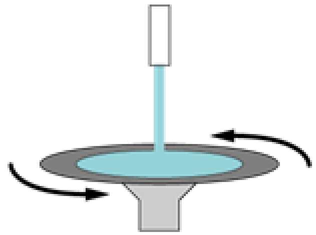
Kovio, Inc.,

Prof. T. Shimoda, JAIST

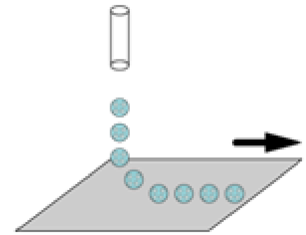
- Reduction of manufacturing cost
- Reduction of environmental load

Printing technology to assemble nano dots

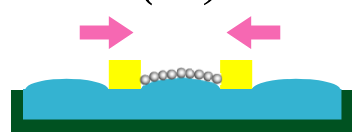
Spin-coating



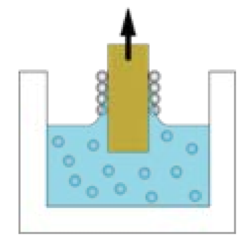
Inkjet-printing



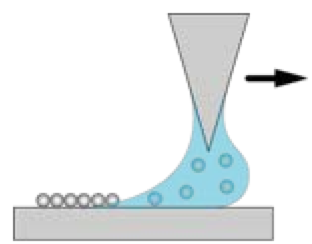
Langmuir-Blodgett (LB)



Dip-coating



Dip-Pen Nanolithography



New fabrication method
New application

Dot Assembly: Summary and Conclusion

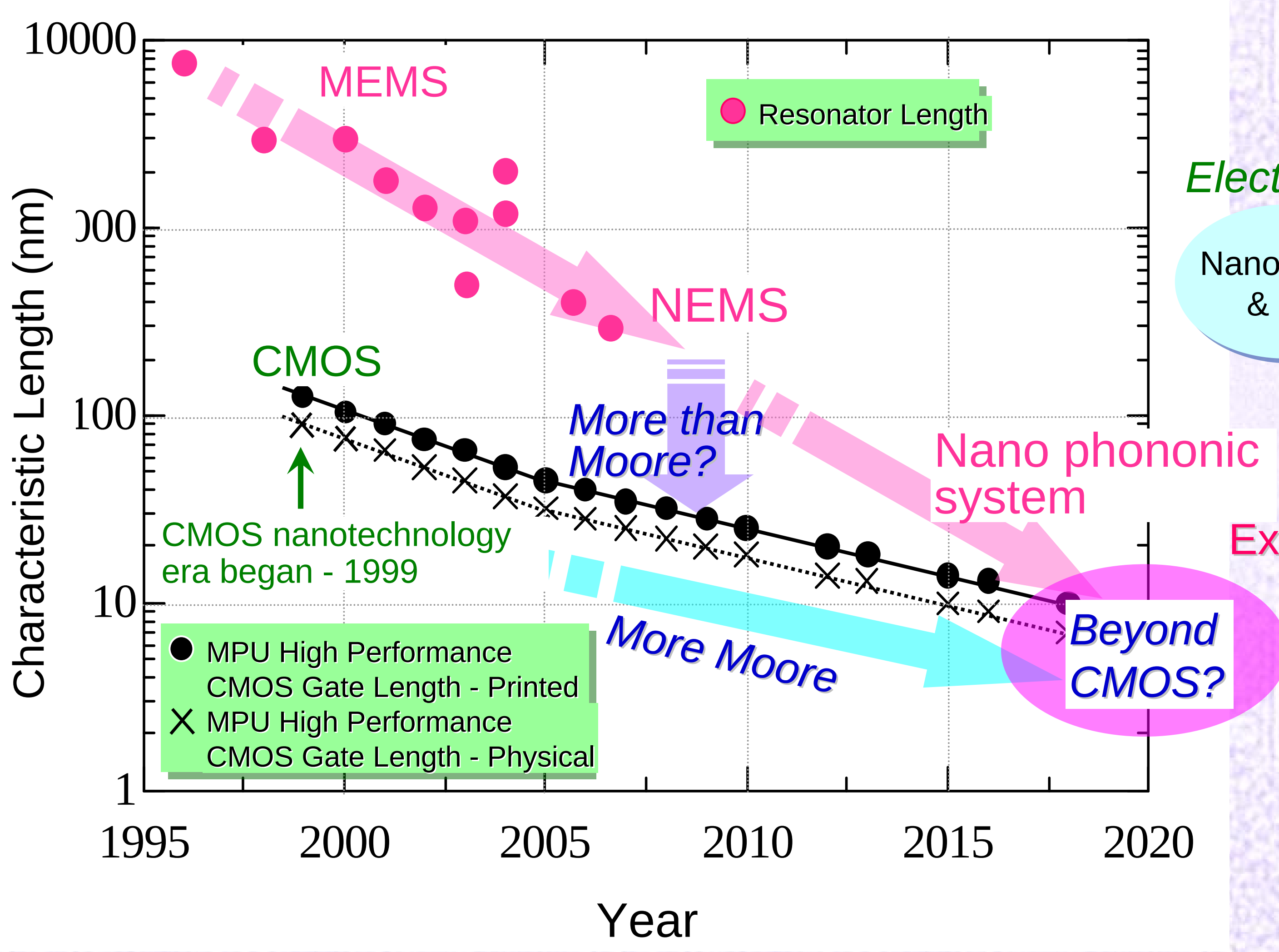
- Fabrication of monodispersed Si nano dots
- Substitutional impurity doping in Si nano dots
- 2D array of Si dots by LB and dip-coating

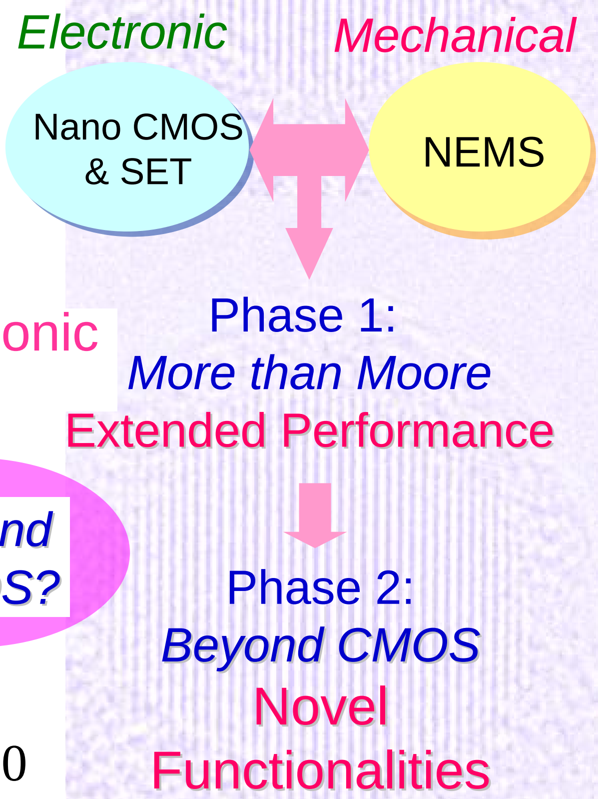
- Surface modification plays key roles in assembly and electron transport.
- Si nanodots in solution are promising for TFTs and photovoltaics.

P-3
P-6
P-7
P-8

NEMS integrated into Si nanodevices

Fusion of NEMS & nano CMOS / SET may lead to extended device performance and even novel functionalities.

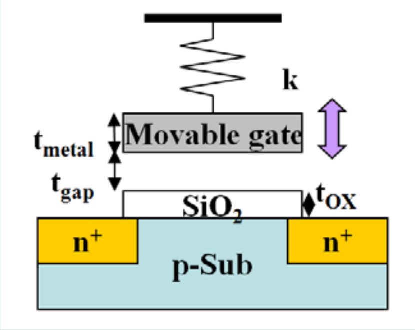


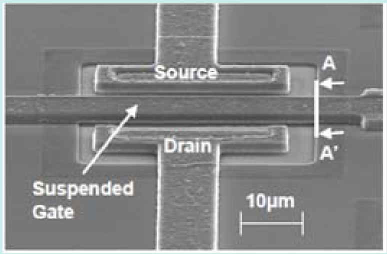


MEMS / NEMS - MOSFET hybrid devices

Switch

Suspended-gate MOSFET



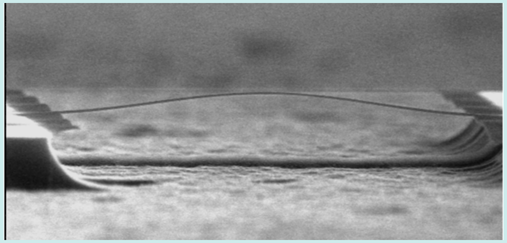


N. Abele *et al.*, IEDM 2005

- Abrupt switching with a subthreshold swing S < 60 mV/dec
- Very low leakage
- Power management

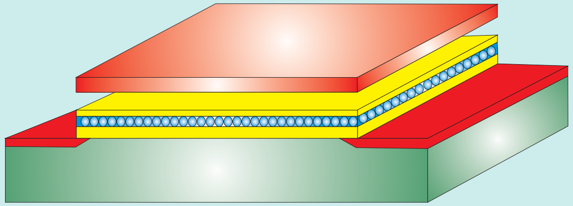
Memory

Self-buckling FG Memory



Y. Tsuchiya *et al.*, J. Appl. Phys. **100** (2006)

SG Si Nanodot Memory

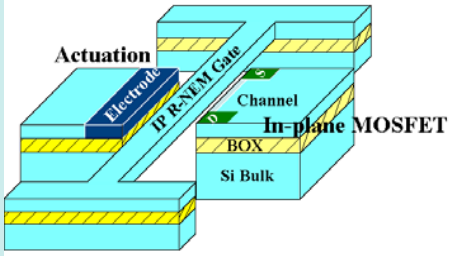


M. Ramirez *et al.*, ESSDERC Fringe (2008)

- Seriously non-volatile
- High-speed write/erase operation
- Conventional silicon process compatible

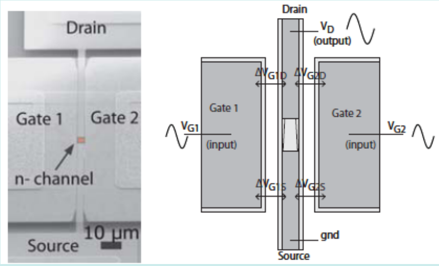
Sensor

Resonant SG MOSFET



F. Hassani et al., submitted to SSDM2009

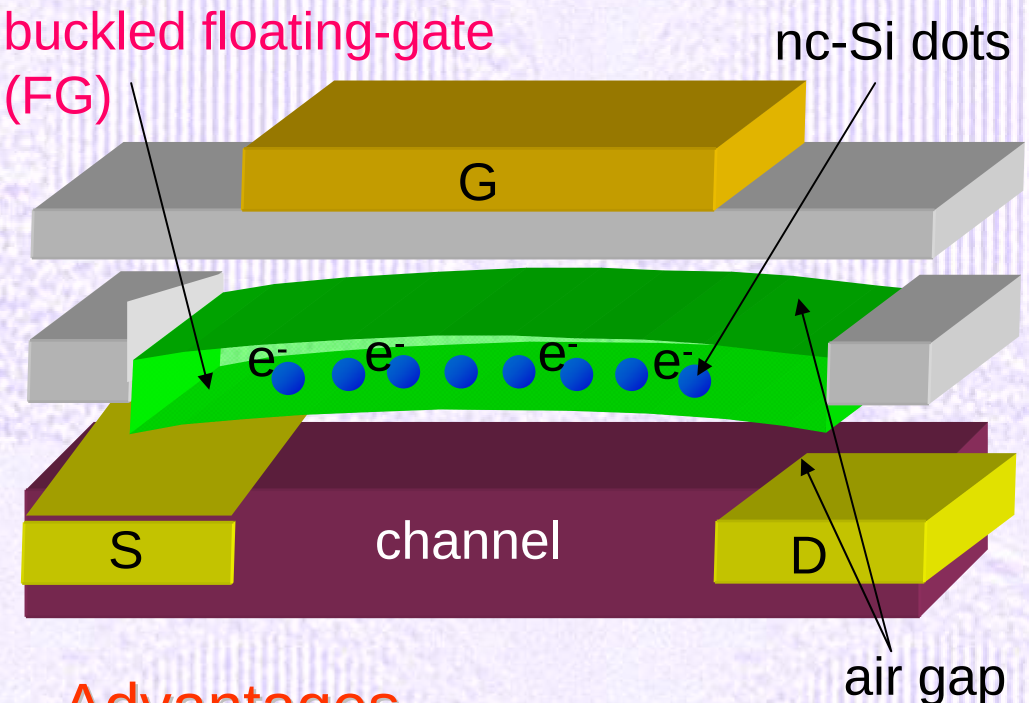
Vibrating body (VB) FET

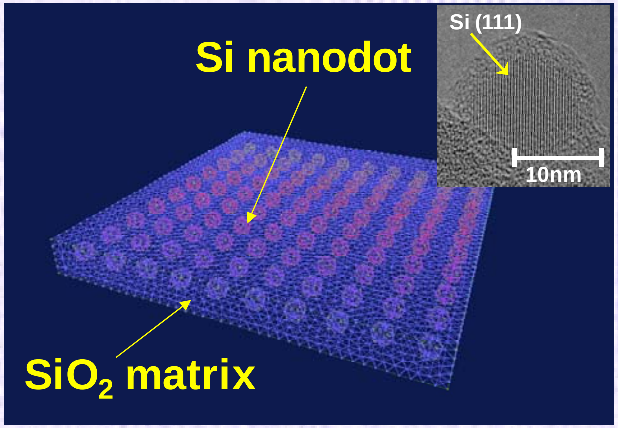


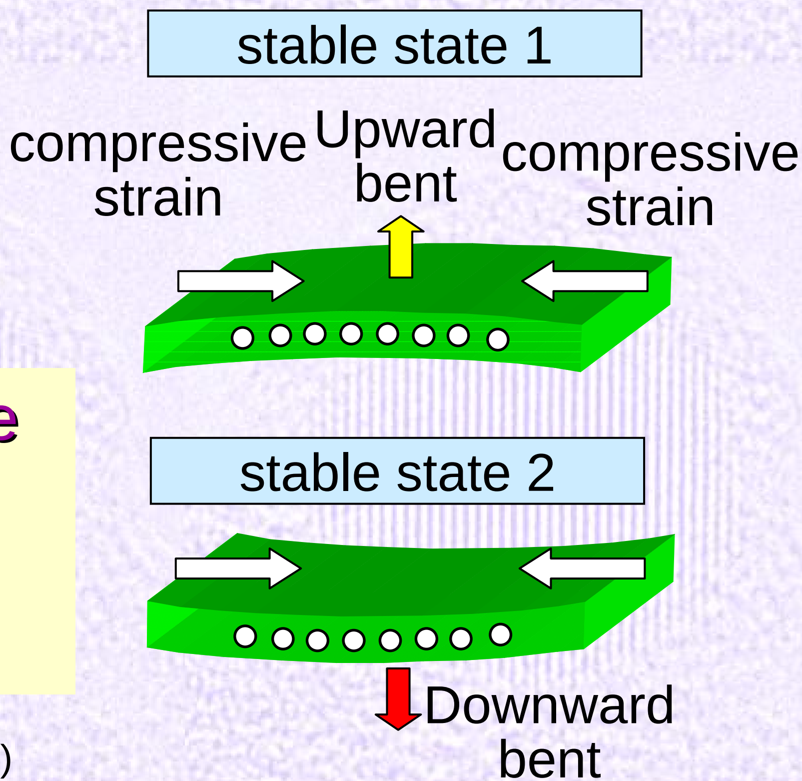
D. Grogg et al., IEDM 2008

- Extremely high mass LOD of sub-attogram order
- Co-integration with SOI-MOSFET circuits

Si-based bistable FG nonvolatile NEMS memory





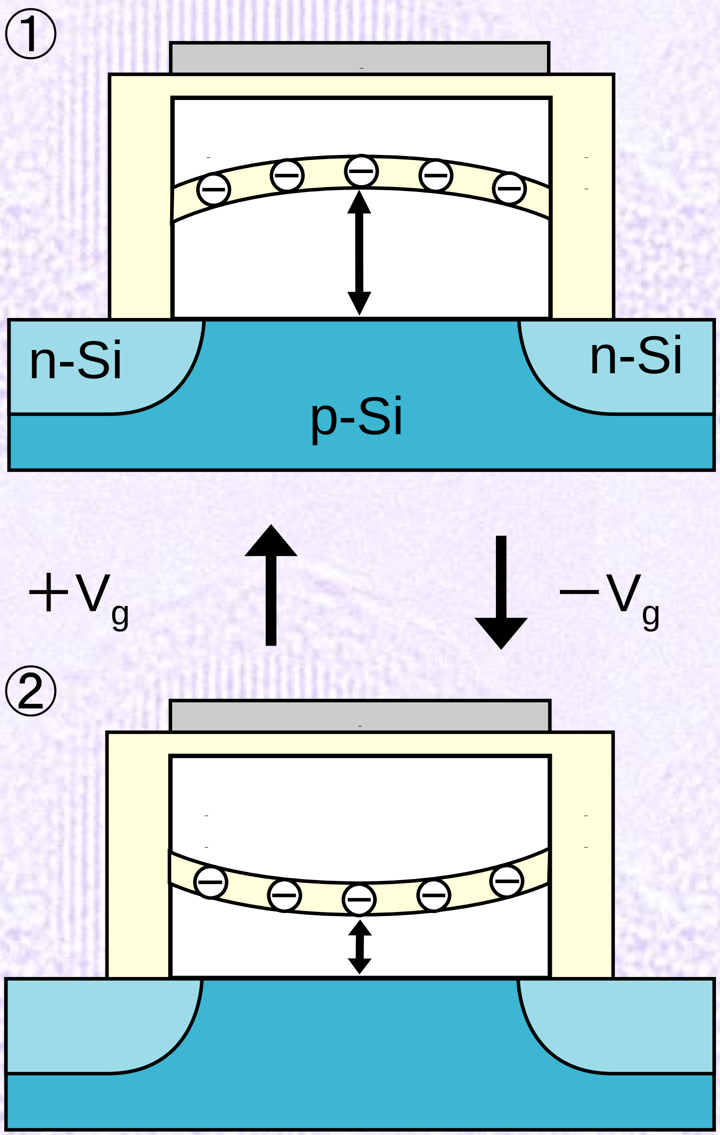


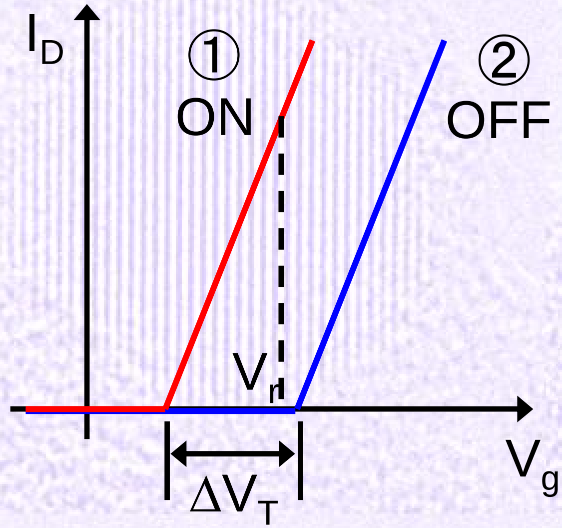
Advantages

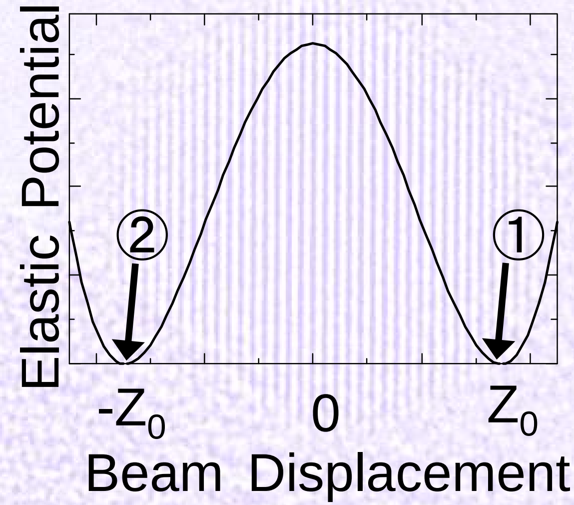
- No charge tunneling via gate oxide
- High-speed write/erase operation
- Compatibility with conventional Si process

J. Appl. Phys. **100**, 094306 (2006), IEEE T-ED **54**, 1132 (2007)

NEMS memory: Operation principle







Write/Erase (switching)

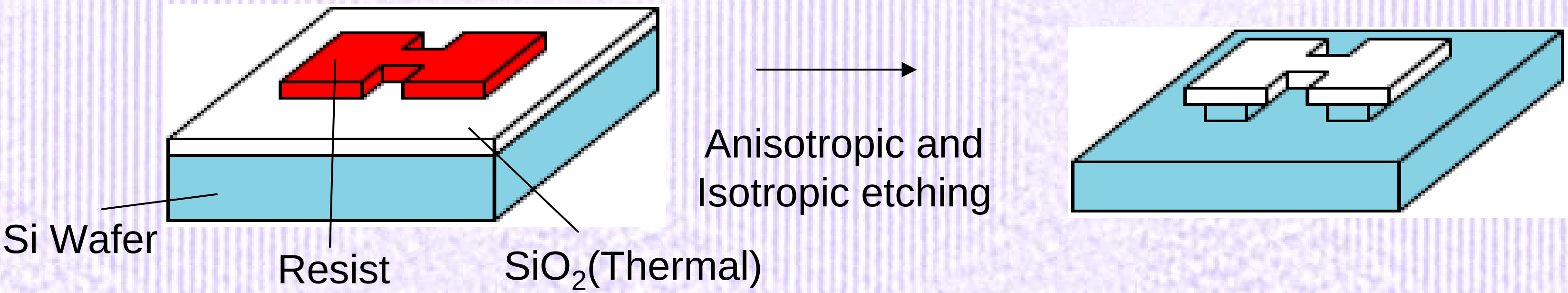
Apply positive or negative gate voltage.

FG moves upward or downward by electrostatic force

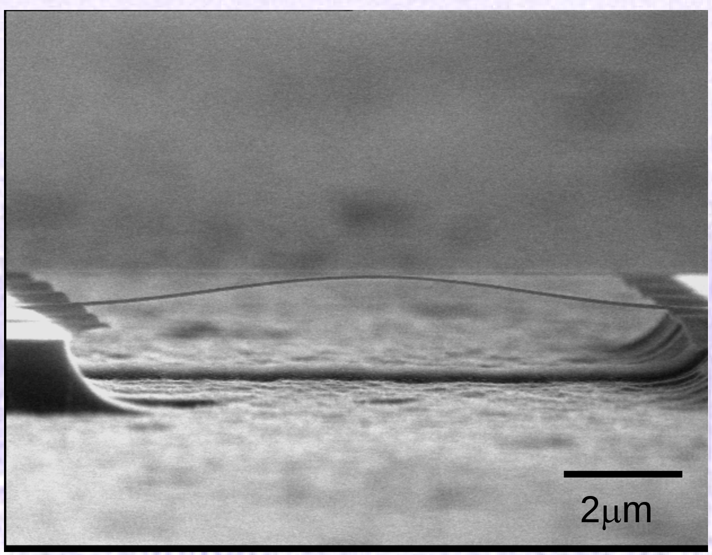
Read state

Difference of distance between FG and substrate causes threshold voltage shift.

Test beam structure fabrication

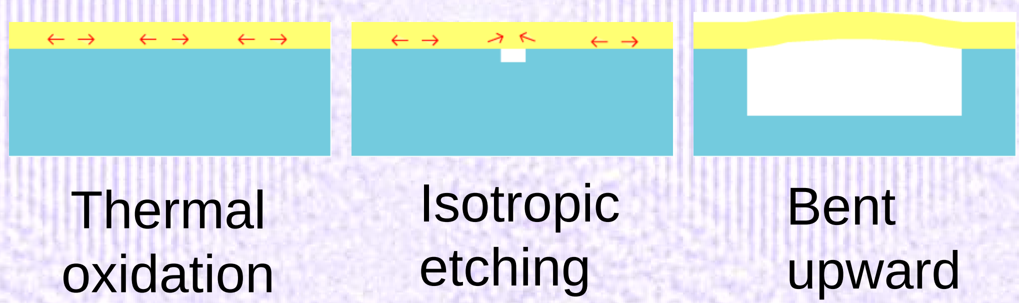


SEM image of a beam



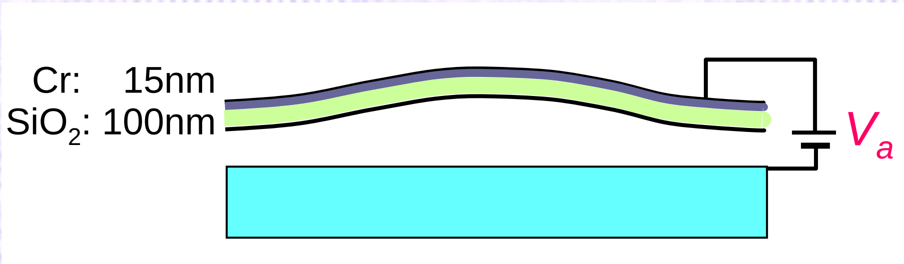
Naturally upward-bent bridge structure observed

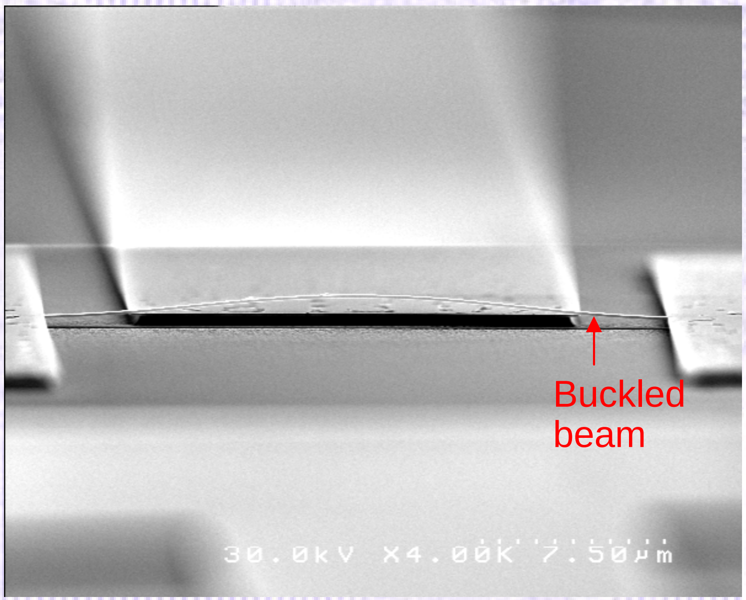
→ Release of stress at Si/SiO_2 interface after undercut



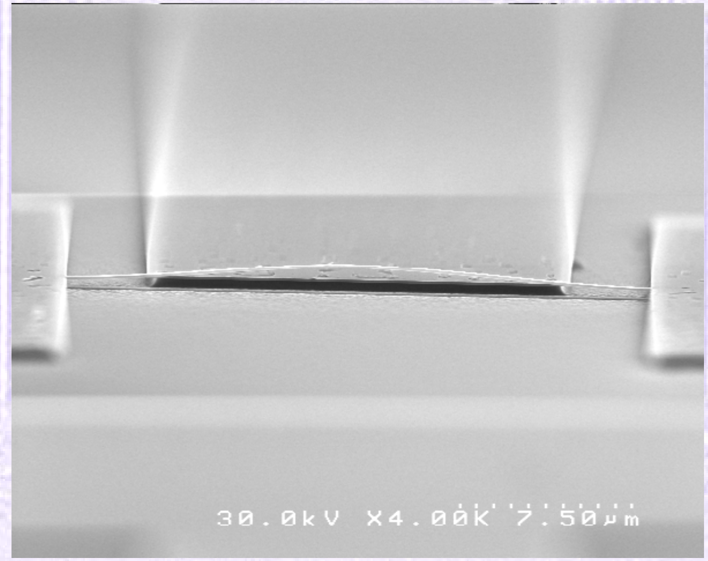
J. Appl. Phys. **100**, 094306 (2006)

Electrical switching of the beam

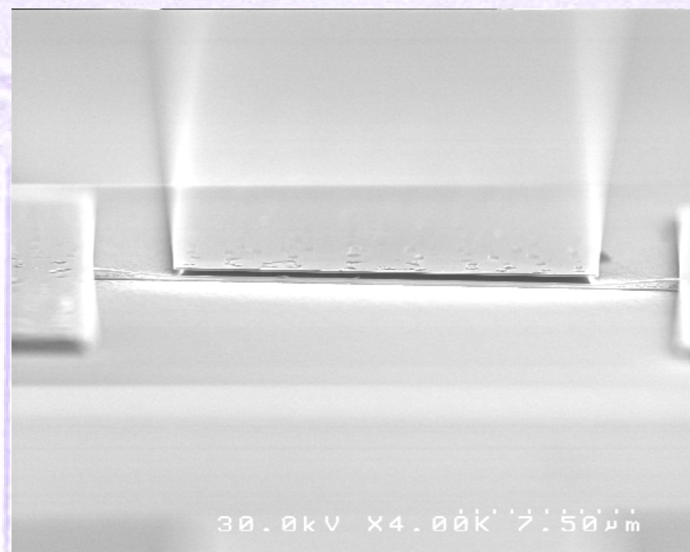




$V_a = 0V$



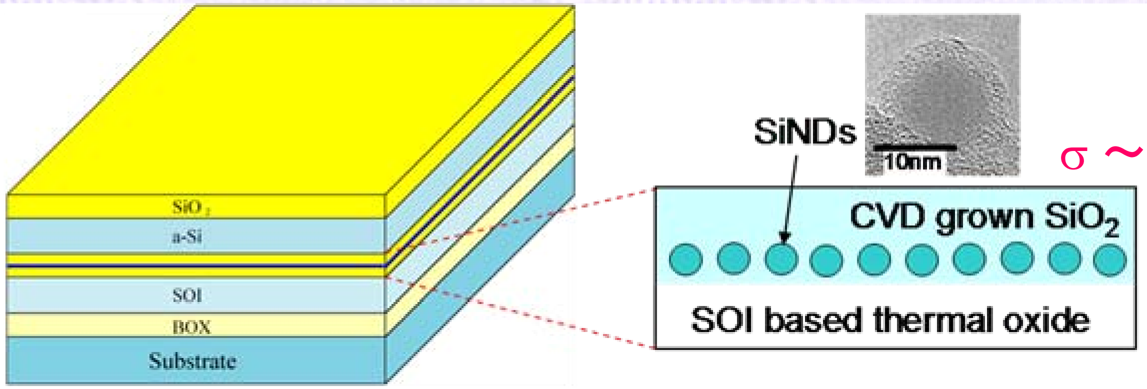
$V_a = 36V$



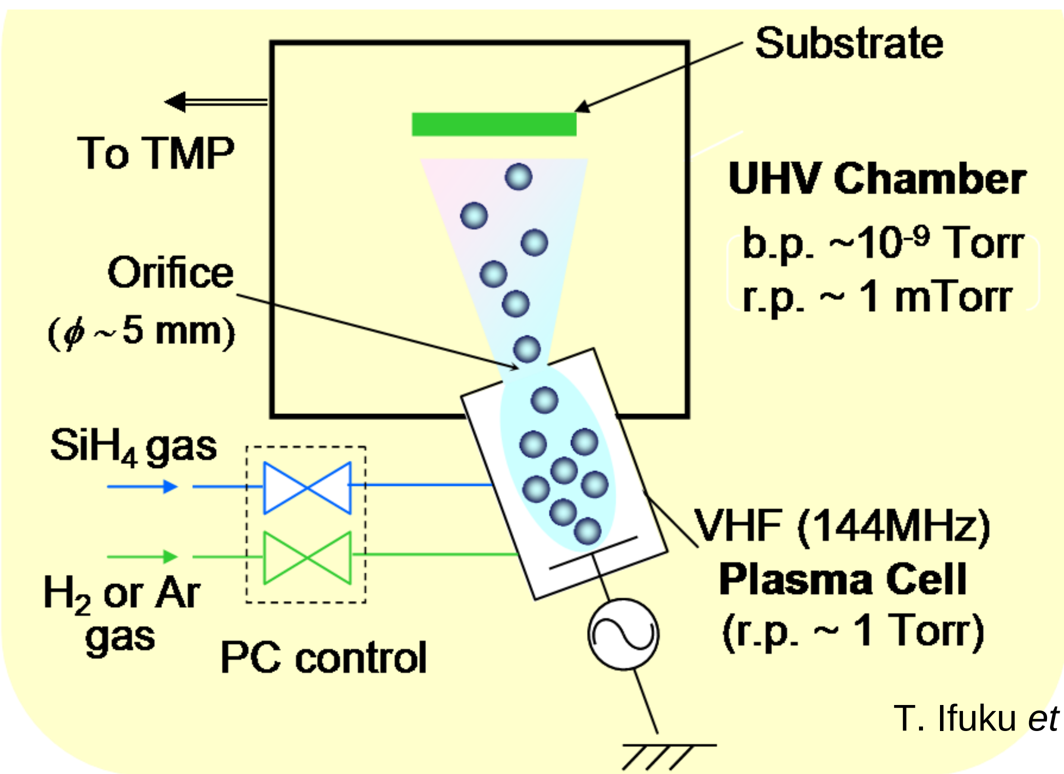
$V_a = 37V$

Mechanical bistability of a self-buckling beam

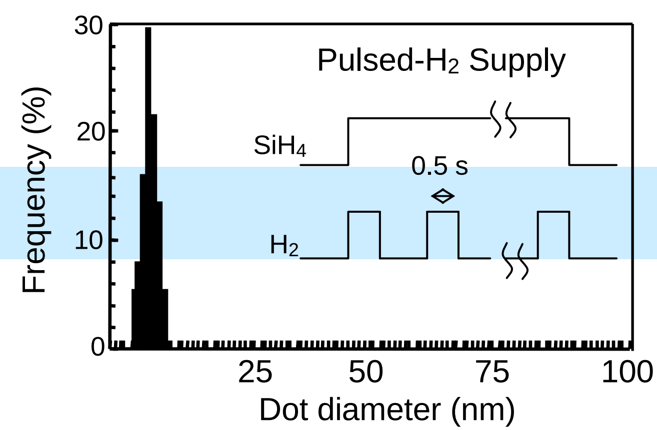
Fabrication of FG with SiNDs



$\sigma \sim 2 \times 10^{11}$ cm^{-2}



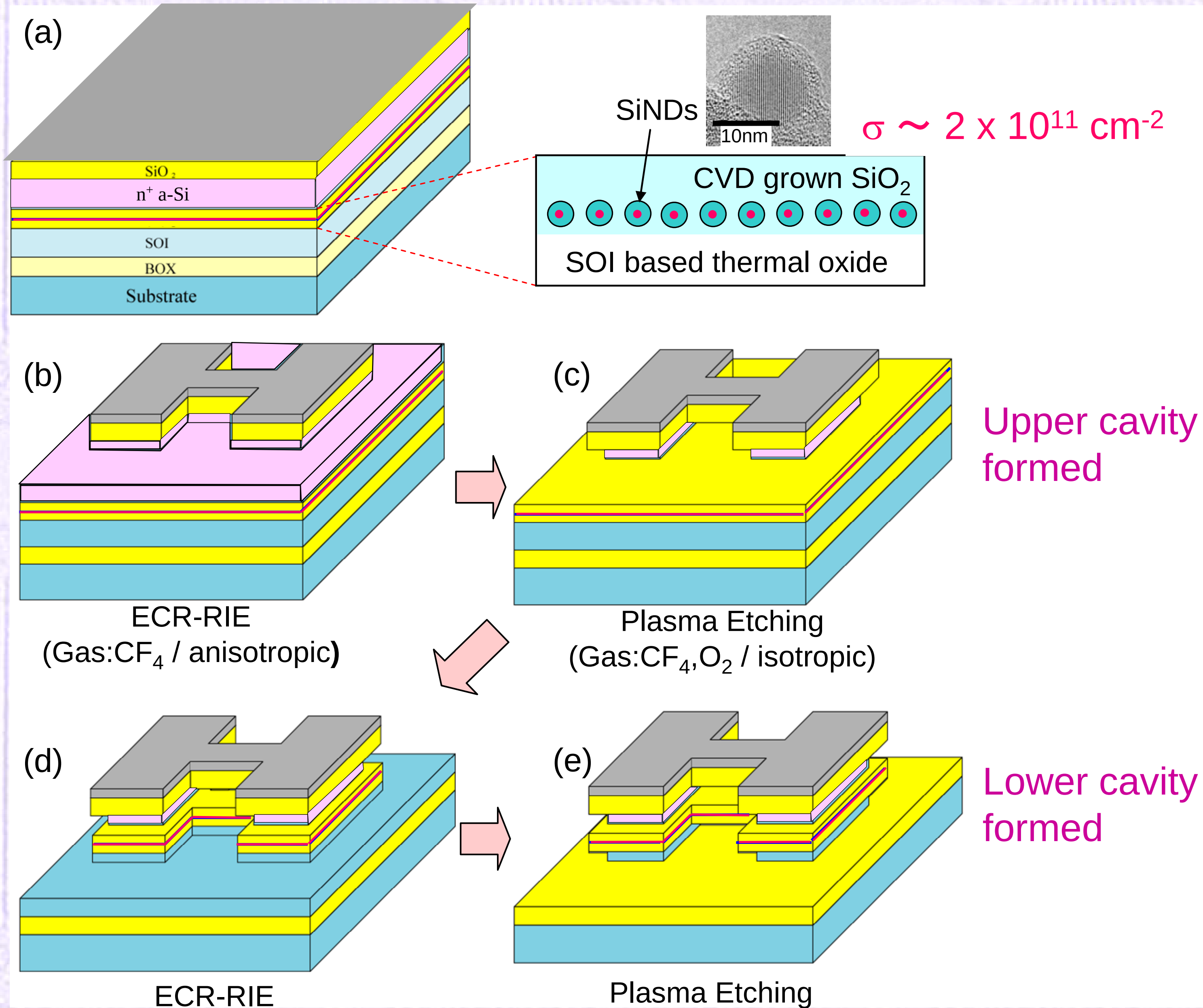
Diameter < 10 nm & dispersion ±1nm



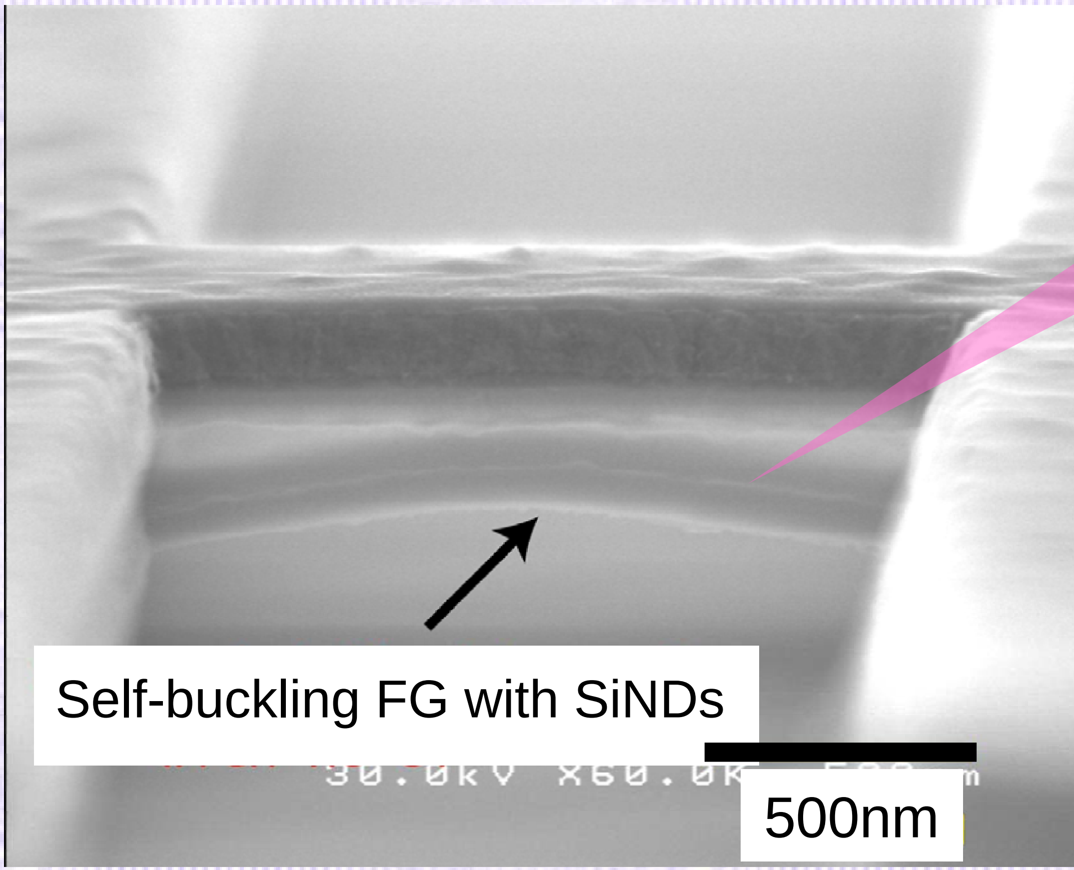
T. Ifuku *et al.*, Jpn. J. Appl. Phys. 36, 4031 (1997)

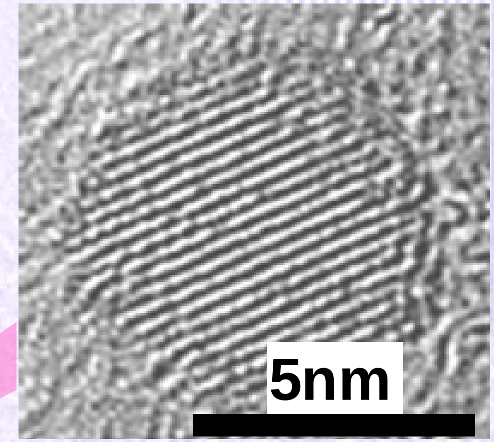
VHF pulsed plasma process: nc-Si dot deposition

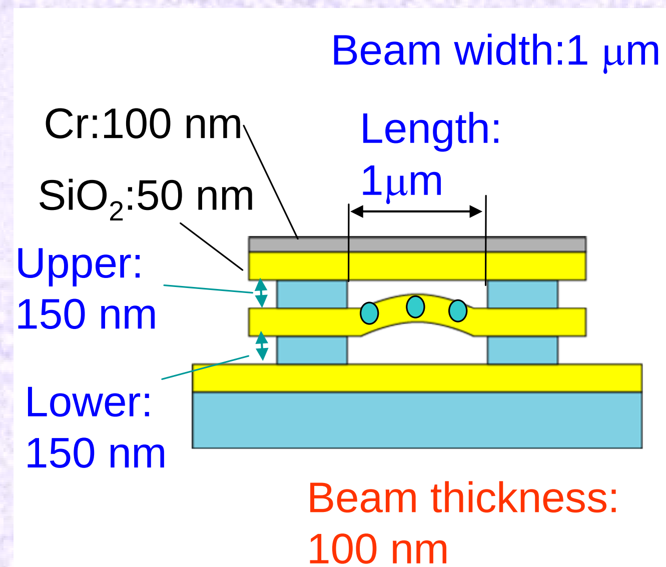
Fabrication of FG with SiNDs



Self-buckling FG with SiNDs



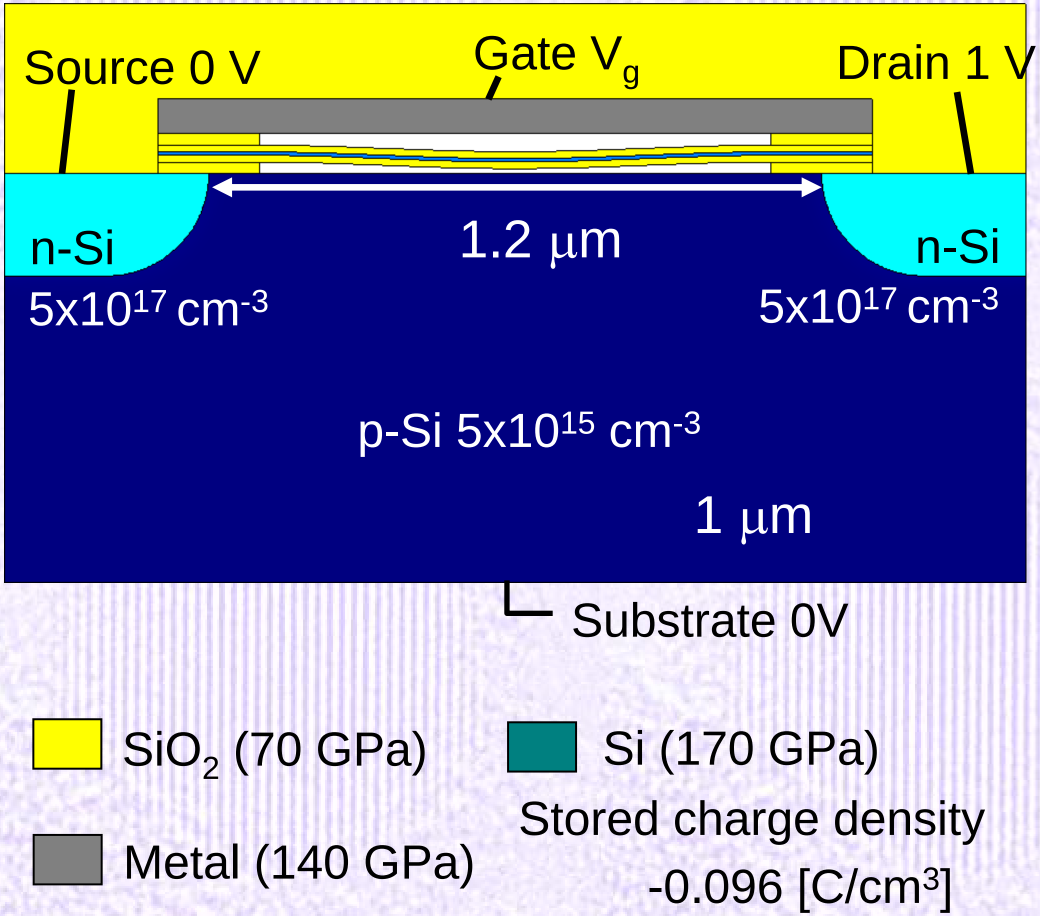




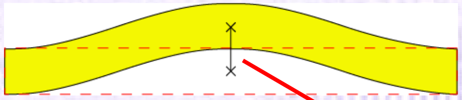
2D simulation of NEMS memory

Finite element method multiphysics simulation

Structural mechanics + Electrostatics + Drift-diffusion



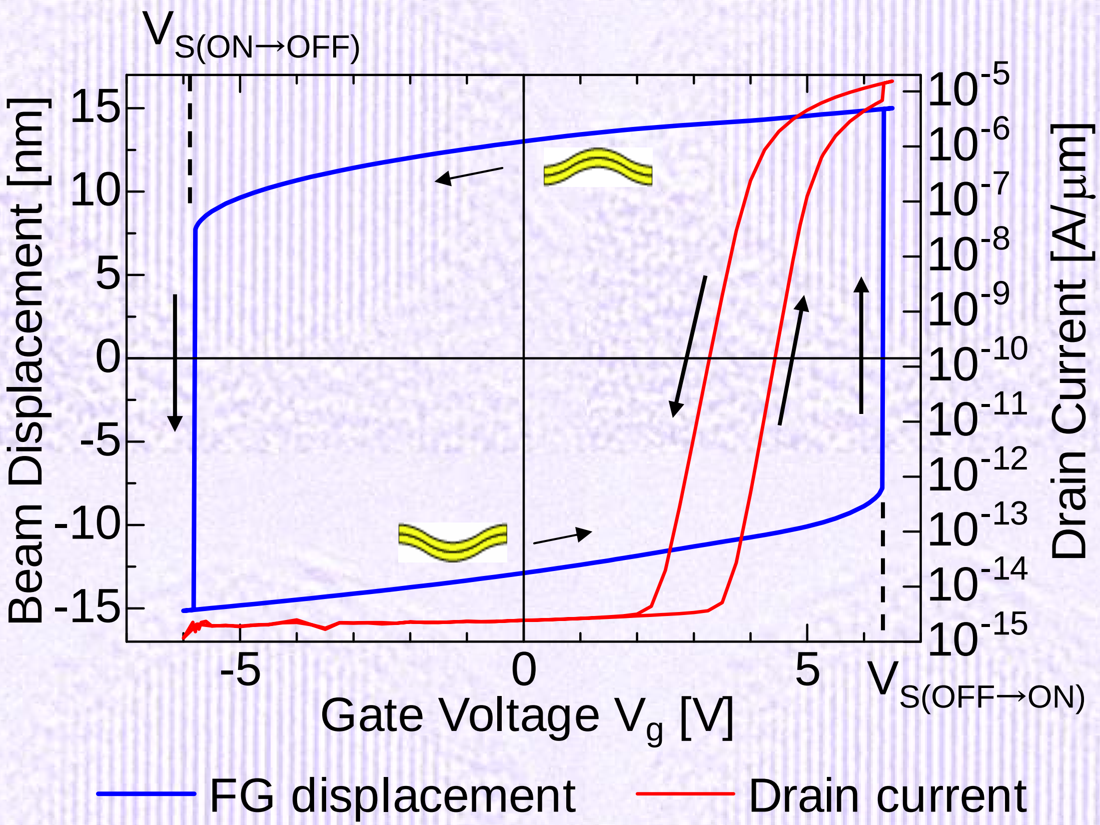
Stored charge density -0.096 [C/cm^3]

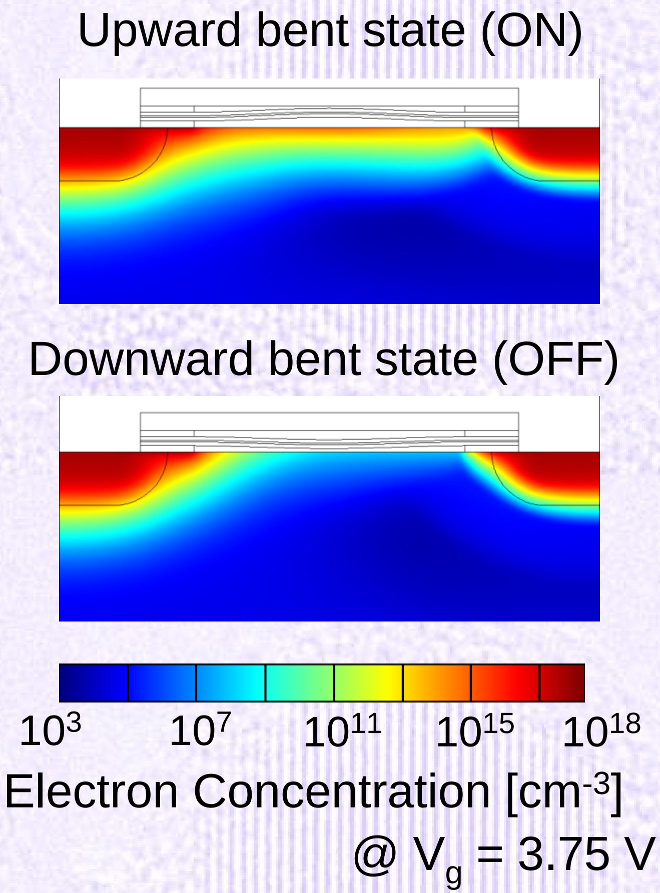


Calculating floating gate displacement and drain current characteristics

$$J = \left(-qn\mu_n \nabla\psi + qD_n \nabla n\right) + \left(-qp\mu_p \nabla\psi - qD_p \nabla p\right)$$

Steady state analysis of NEMS memory

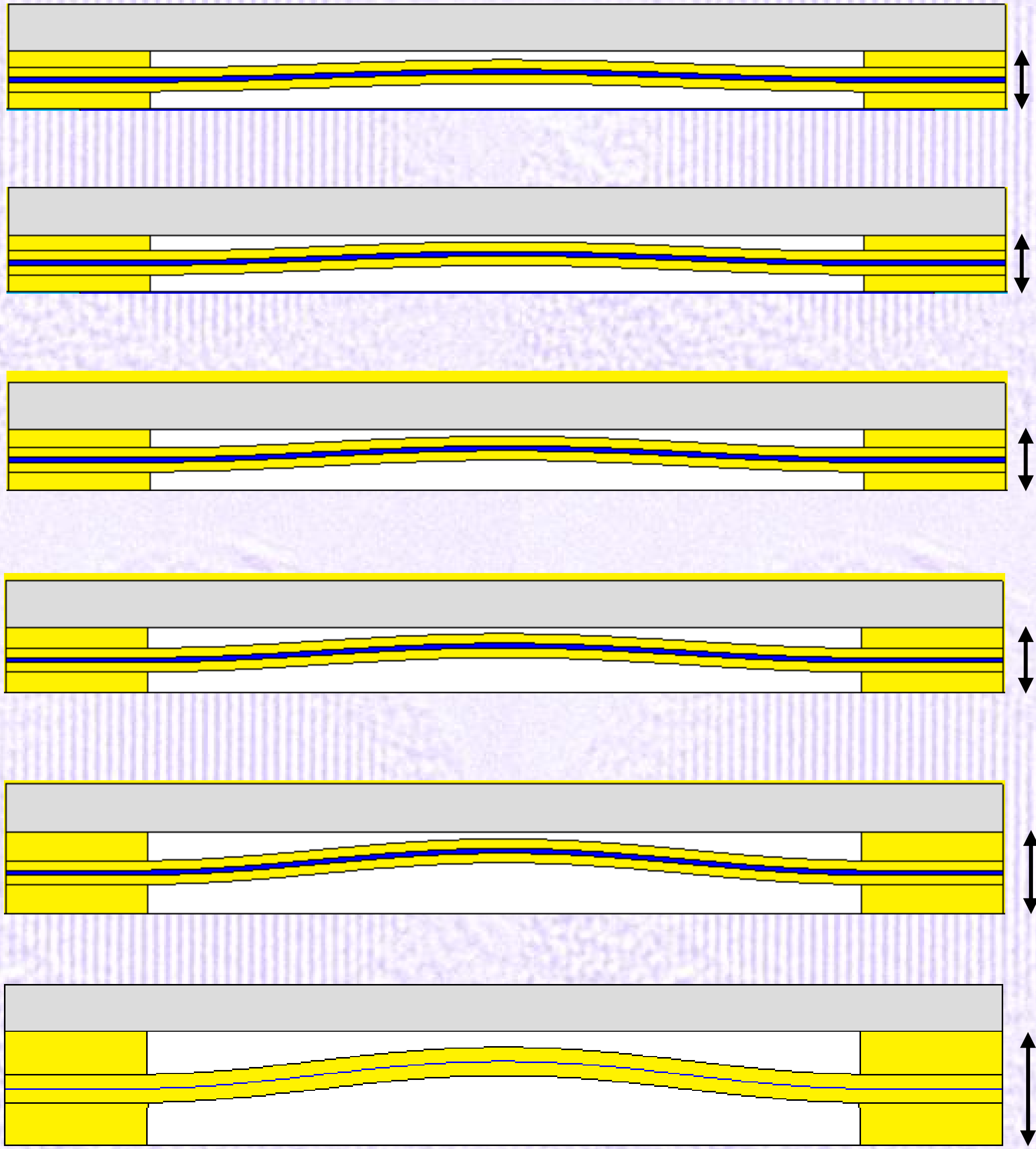




Floating gate can be switched by applying gate voltage.

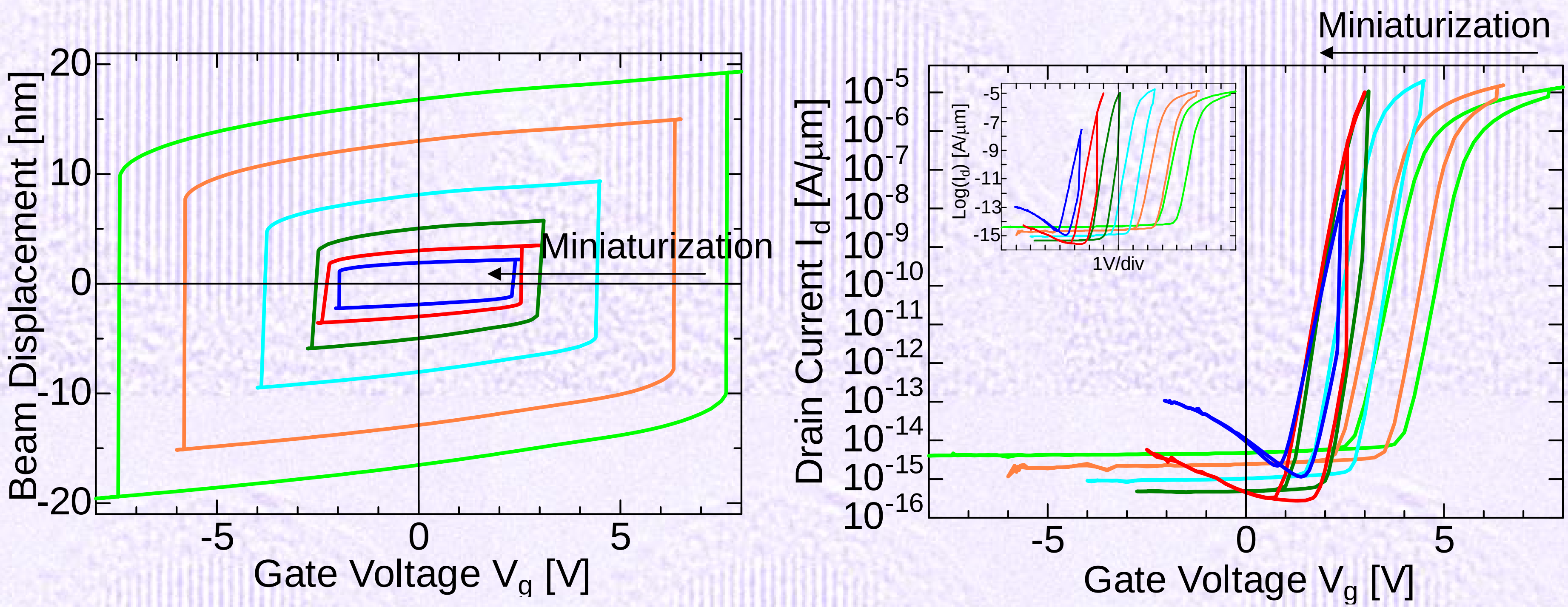
Drain current changes by position of floating gate.

Simulated structures



	FG length
120 nm	1.5 μm
79.3 nm	1 μm
41.7 nm	500 nm
22.3 nm	250 nm
12.7 nm	100 nm
8 nm	50 nm

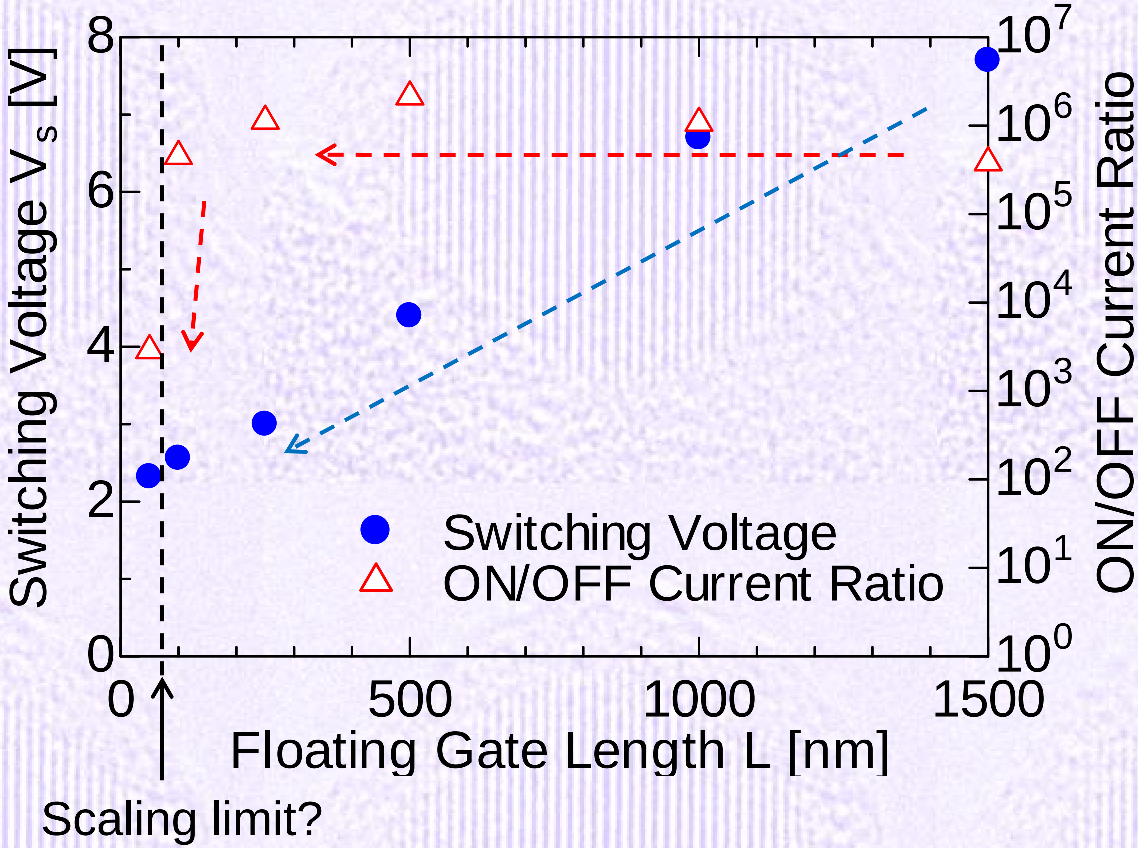
Beam displacement and drain current characteristics



Floating gate length

50nm 100nm 250nm 500nm 1000nm 1500nm

Memory property changes by scaling



Switching voltage decreases with size reduction.

Current ratio is maintained 10^5~10^6 until L = 100 nm.

Transient simulation for P/E time estimation

$$\rho\frac{\partial^2\mathbf{u}}{\partial t^2}+\xi\frac{\partial\mathbf{u}}{\partial t}-\nabla\cdot(\mathbf{c}\nabla\mathbf{u})=\mathbf{F}$$

Damping term

Rayleigh damping model

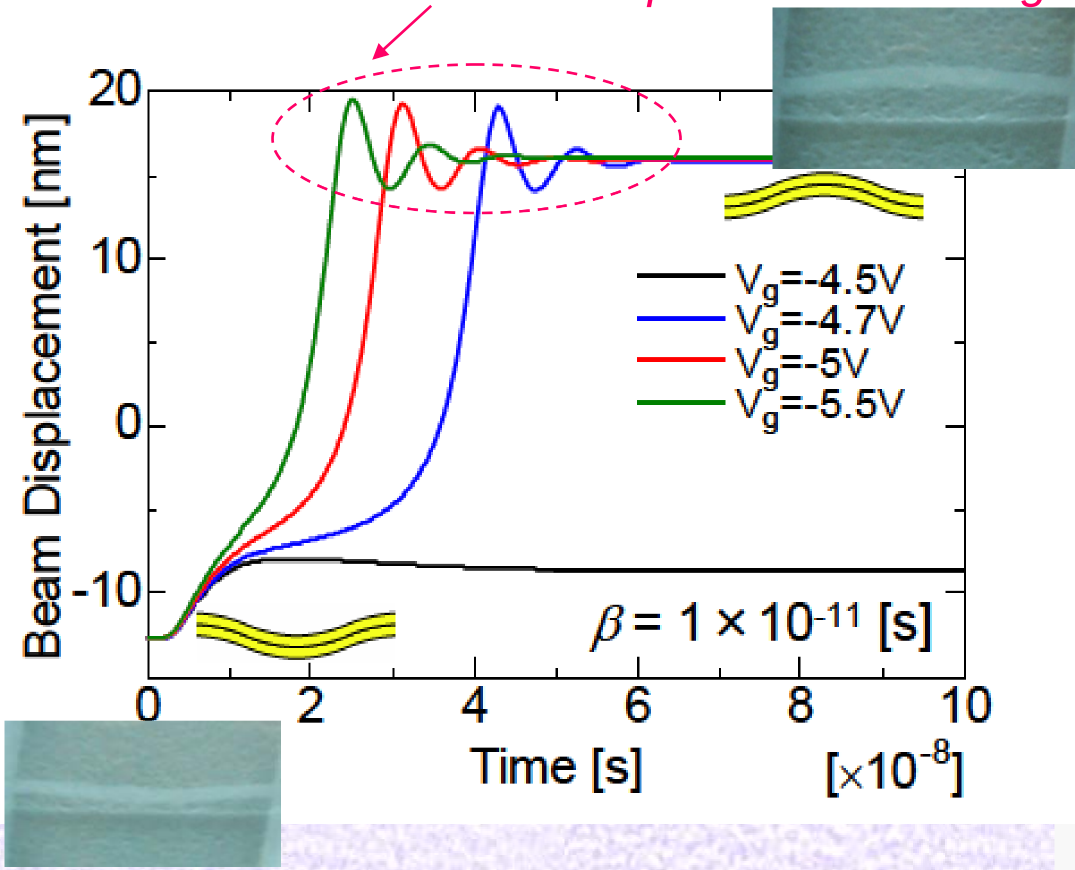
$$\xi=\alpha\,m+\beta\,k$$

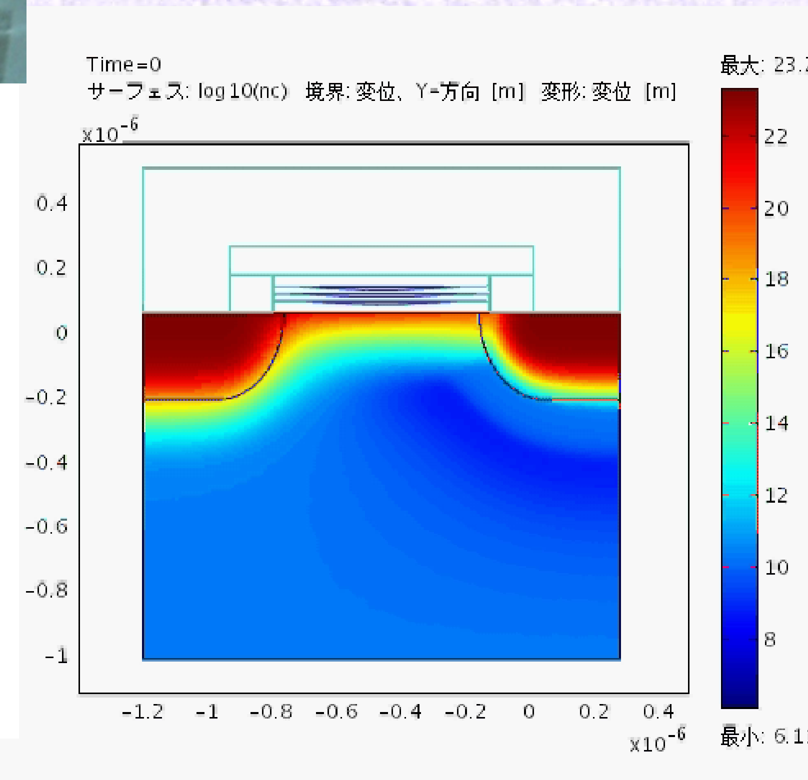
mass damping — stiffness damping

For FG length of 1 μm

- ON -> OFF : 55 nsec
- OFF -> ON : 50 nsec

Beam oscillation dumped after switching

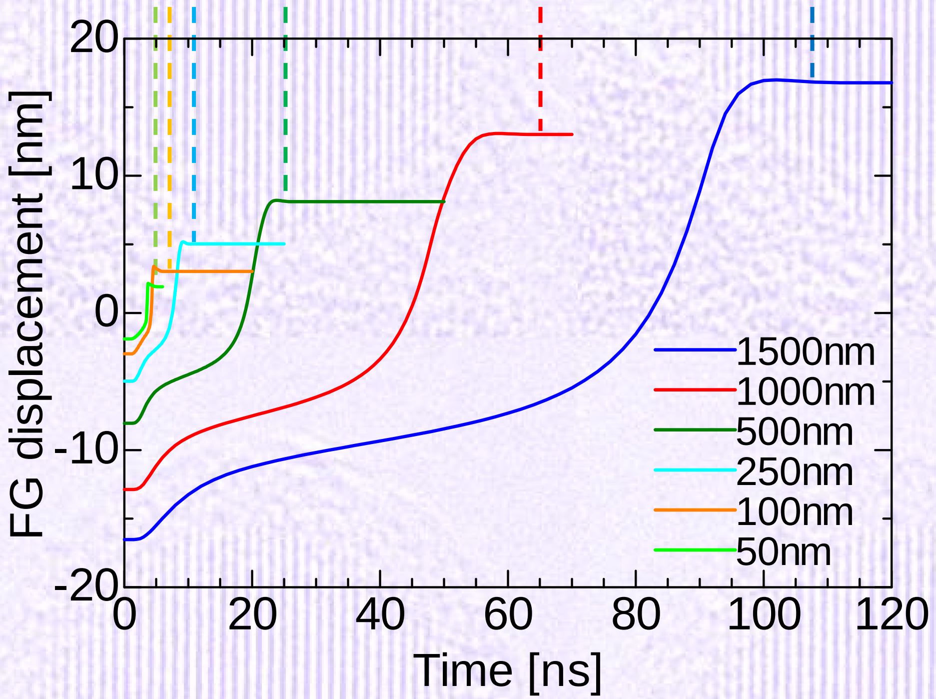


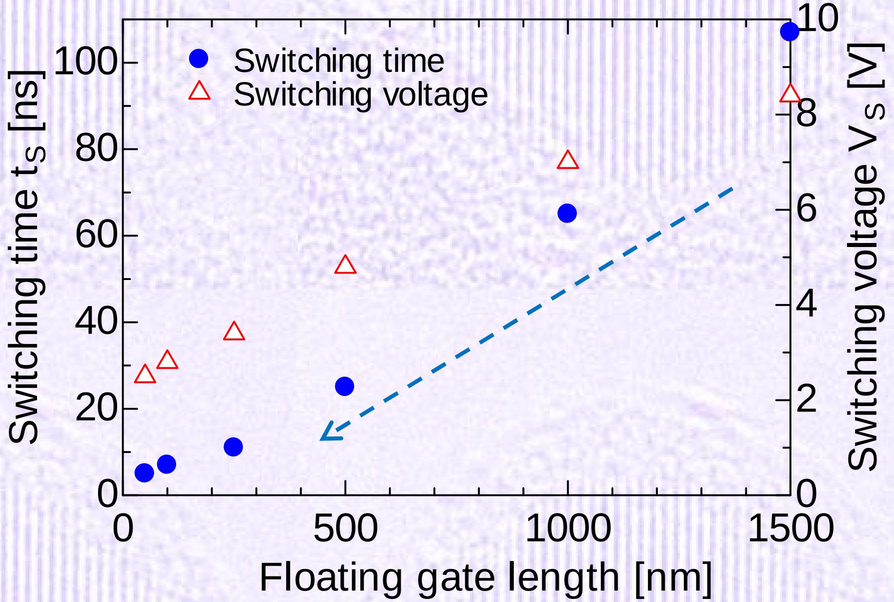


Transient response and switching time

Applying pulse voltage and calculating switching response

(Assuming ideal damping factor for each structure)





Switching time decreases with size reduction.

Switching time 7 ns @ L100 nm, V_g2.8 V

Estimation of energy consumption

Estimating energy consumption from total energy

$$E_{sum} = E_m + E_k + E_d + E_e + E_R$$

Mechanical energy

$$E_m = \int_V \frac{1}{2}\varepsilon \cdot \sigma dV = W \times \int_S \frac{1}{2}\varepsilon \cdot \sigma dS$$

σ : stress ε : strain

Kinetic energy

$$E_k = \int_V \frac{1}{2}\rho \mathbf{v}^2 dV = W \times \int_S \frac{1}{2}\rho \mathbf{v}^2 dS$$

Electrostatic energy

$$E_e = \int_V \frac{1}{2}\mathbf{E} \cdot \mathbf{D} dV = W \times \int_S \frac{1}{2}\mathbf{E} \cdot \mathbf{D} dS$$

Damping loss

$$E_d = \int_V \int_0^t \mathbf{F}_d \cdot \mathbf{v} dt dV$$
$$= W \times \int_S \int_0^t \left(\alpha\rho \mathbf{v}^2 + \beta \frac{\partial \sigma}{\partial t} \cdot \frac{\partial \varepsilon}{\partial t} \right) dt dS$$

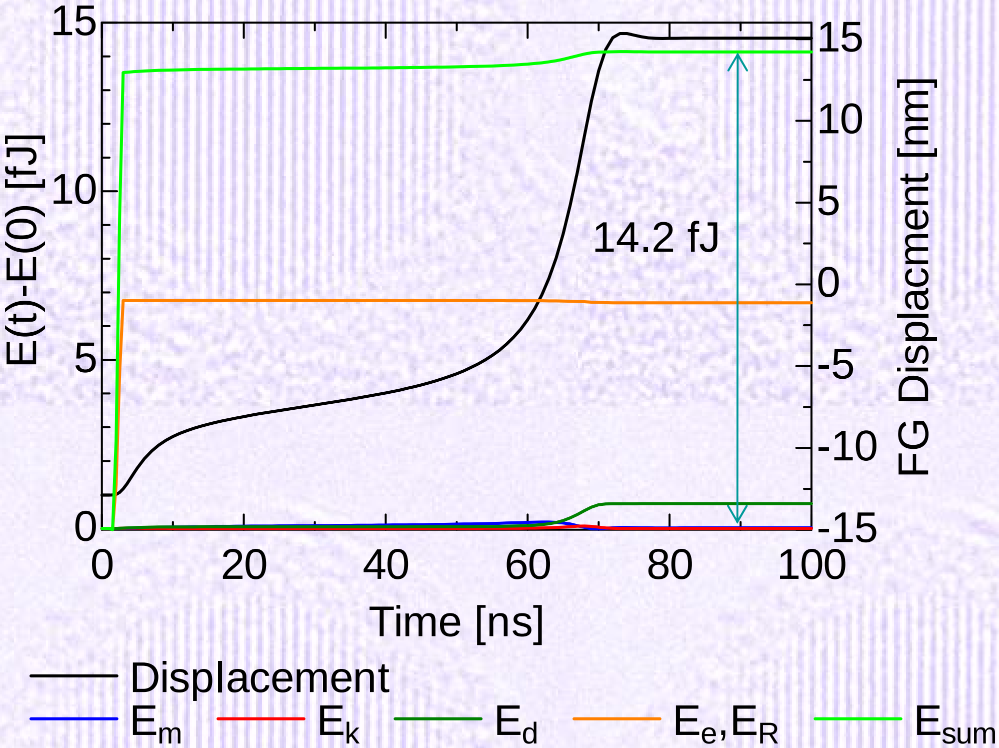
α: mass damping factor
β: stiffness damping factor

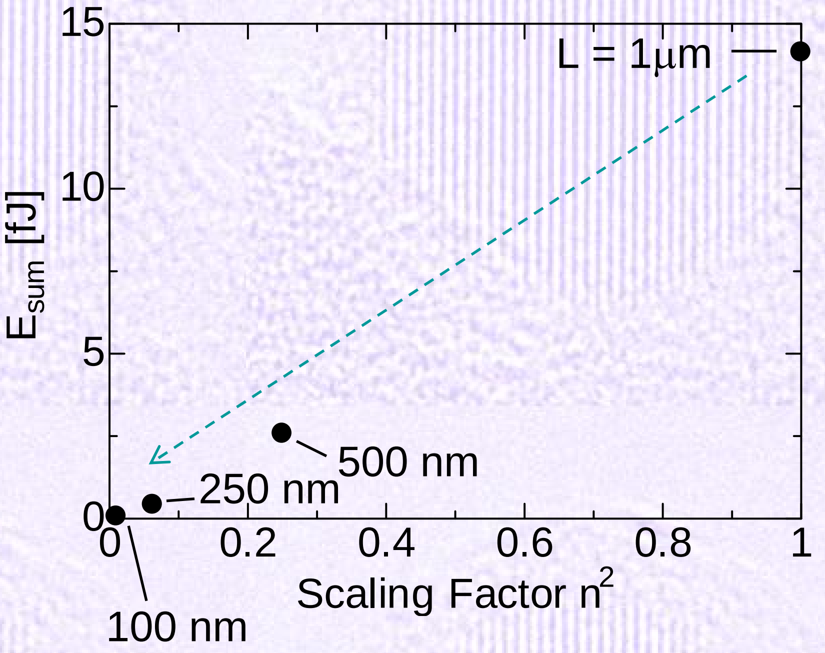
Charging loss

$$E_R = E_e(t) - E_e(0)$$

Switching energy variation by scaling

V_g 6.7 V step voltage (L = 1 μm)





E(t=0)

E_m: 31.5 fJ, E_e: 0.73 fJ, E_k,E_d,E_R: 0 fJ

Size reduction

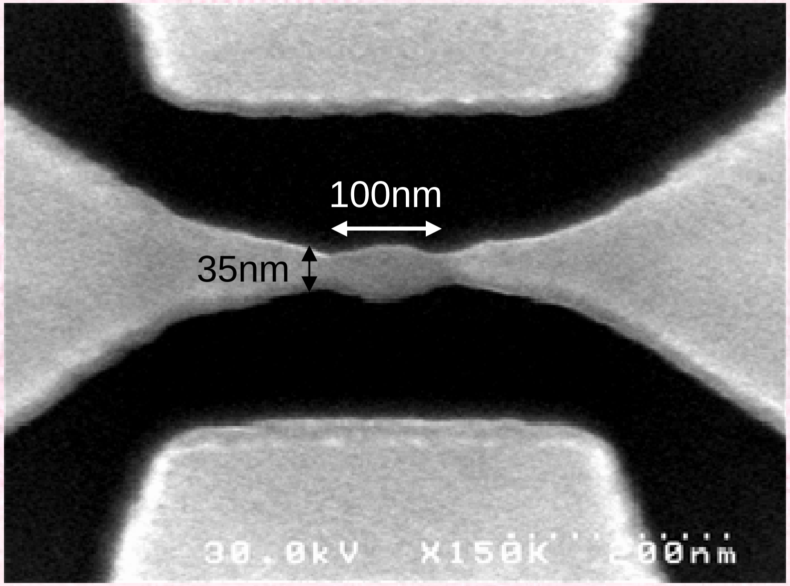
Low energy consumption

(0.07 fJ? @ L100nm)

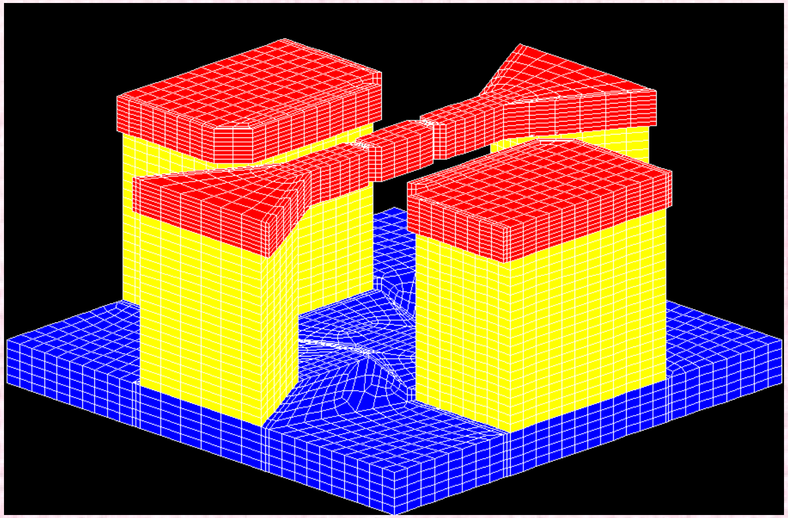
NEMS Memory: Conclusion

- We have performed numerical simulation of NEMS memory devices featuring mechanical bi-stability as a memory node.
- Memory performances enhance with decreasing suspended floating gate length L from 1000nm to 100nm, where switching voltage of 2.5V, switching speed of 15ns, and switching energy of 0.2fJ are projected.
- However, at 50nm, memory window collapses in this device structure. Although not suitable for ultra large scale integration, the fast and ultra low power NEMS memory, which does not require current flow for switching, may find suitable application in mobile terminals.
- Alternative structure, e.g., CNT, may extend scalability.

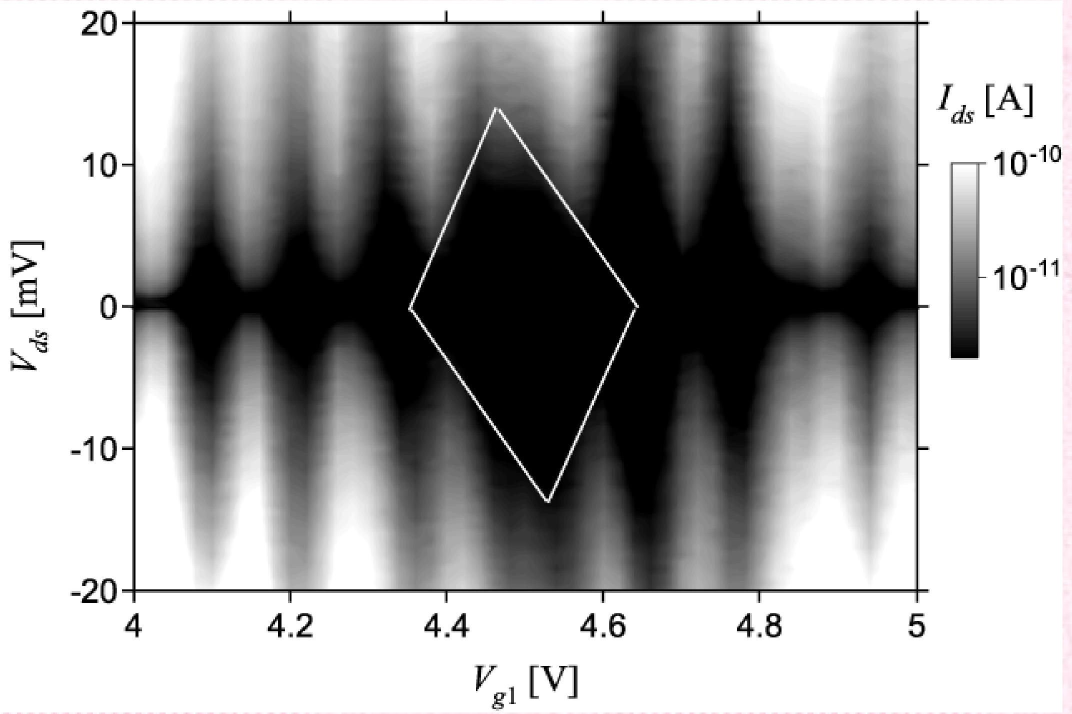
NEMSET: a suspended QD free from substrate



SiNB with a single QD cavity



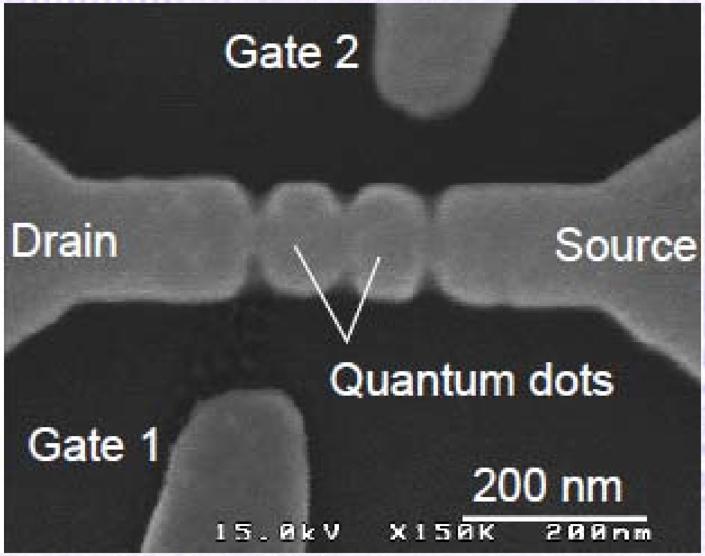
- *Reduced self-capacitance*
- *Acoustically isolated from substrate*



Coulomb oscillation observable at T > 100 K
Unintentionally formed dot(s) included

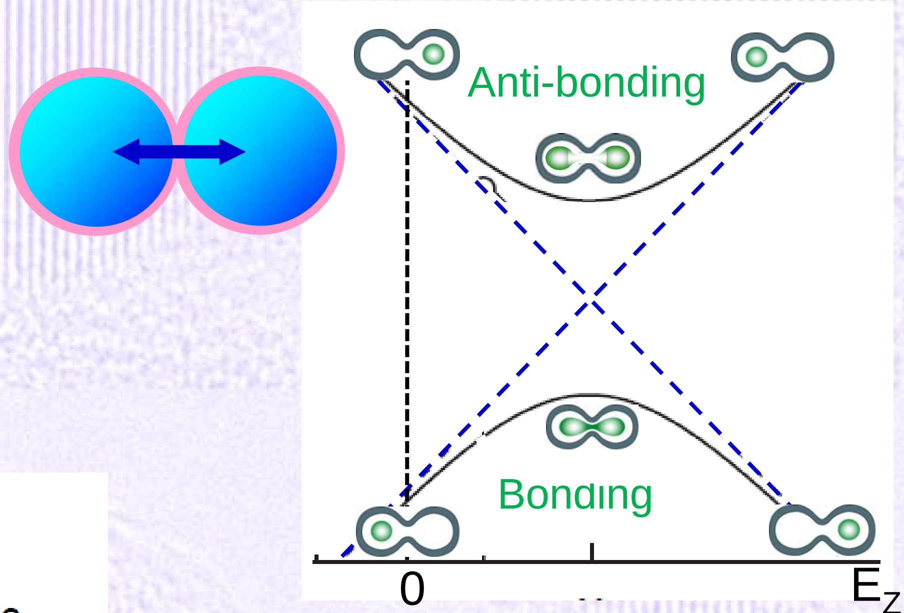
J. Ogi, Y. Tsuchiya, S. Oda and H. Mizuta, Microelectronics Eng. **85**, 1410 (2008)

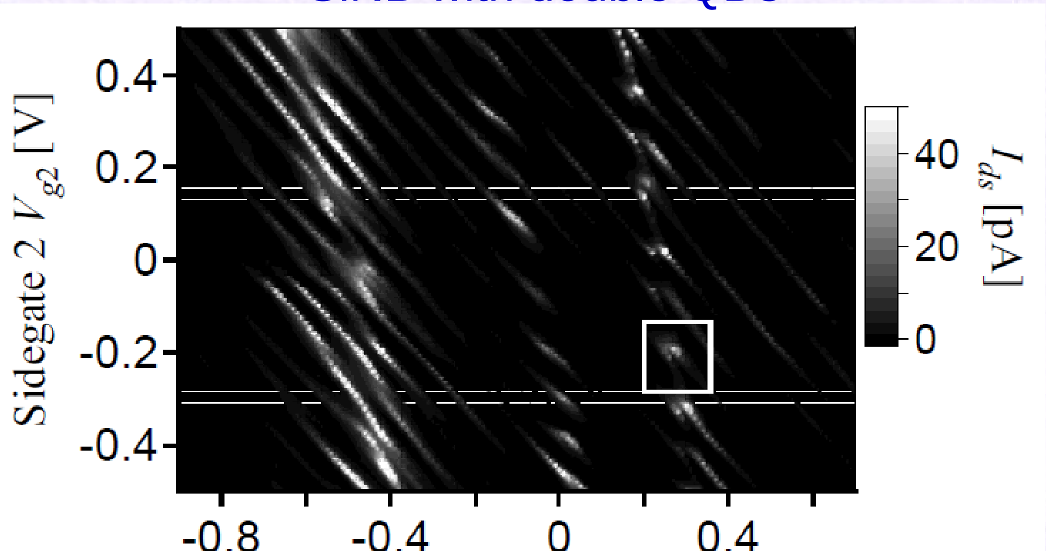
NEMSET : suspended double QDs (SDQDs)

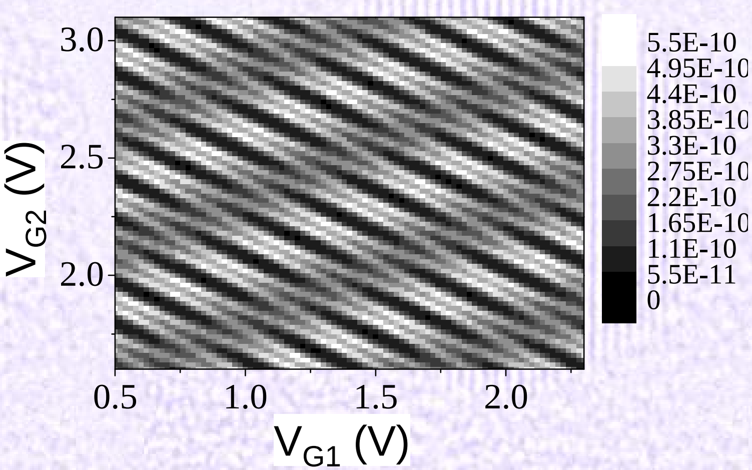


SiNB with double QDs

Charge qubits in an acoustically controlled environment

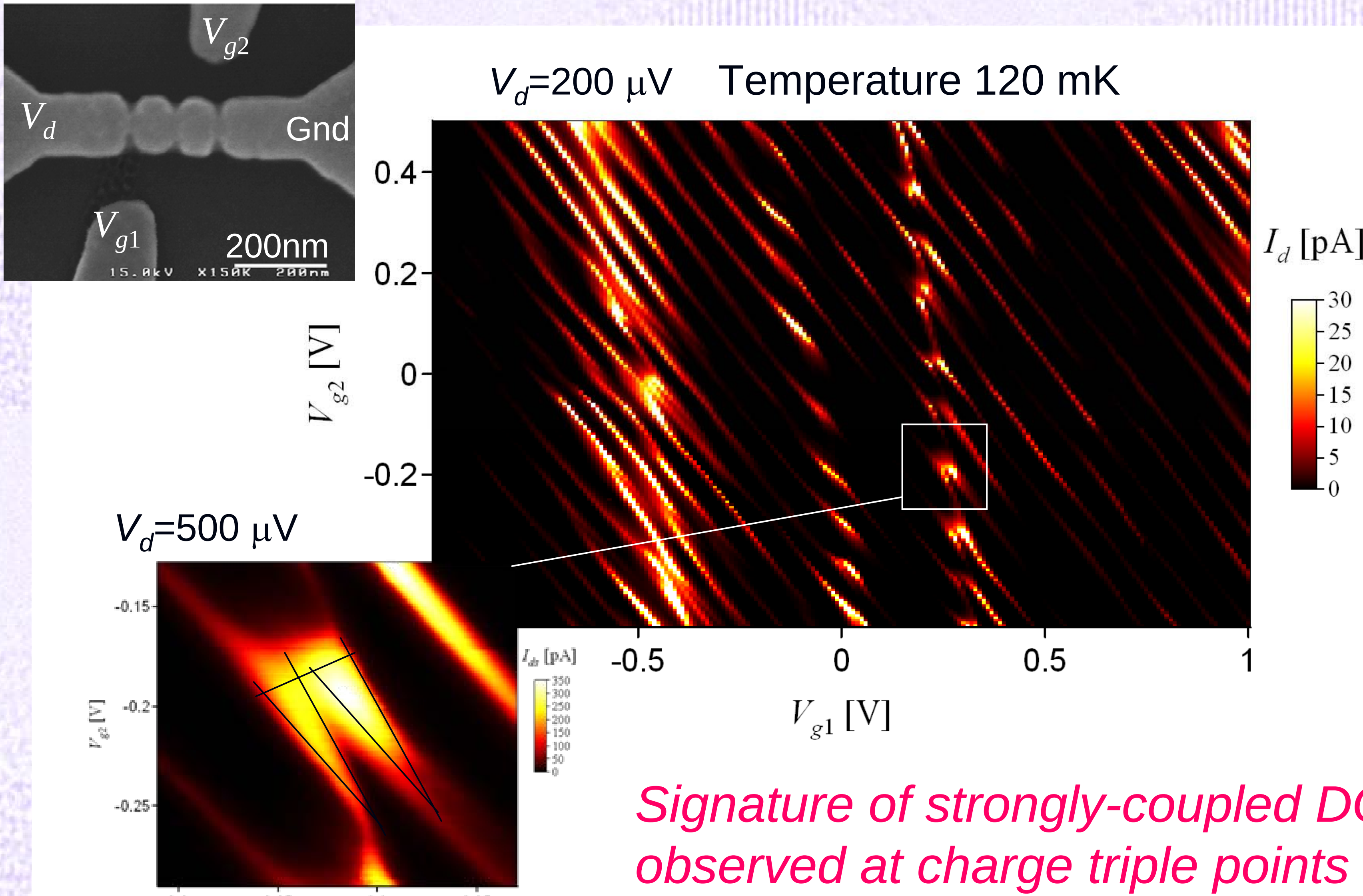






J. Ogi, *T. Ferrus, Y. Tsuchiya, K. Uchida, D. A. Williams, S. Oda and H. Mizuta,* Silicon Nanoelectronics WS, Kyoto, June, 2009

Signature of strongly-coupled SDQDs

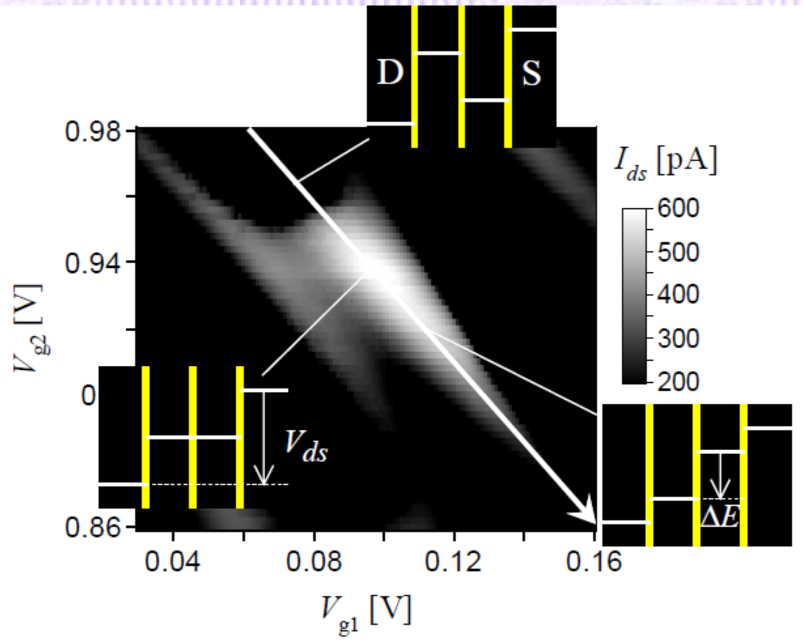


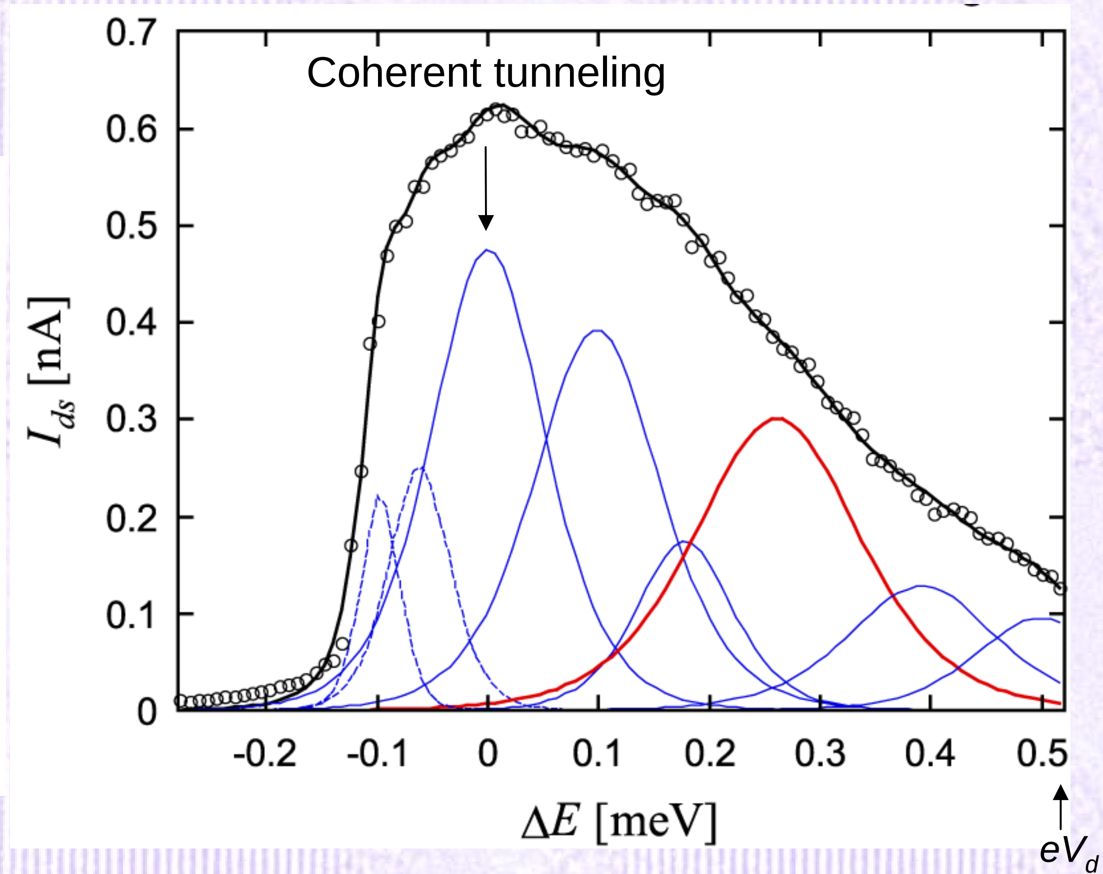
Signature of strongly-coupled DQD observed at charge triple points

J. Ogi, *T. Ferrus, Y. Tsuchiya, K. Uchida, D. A. Williams, S. Oda and H. Mizuta,* Silicon Nanoelectronics WS, Kyoto, June, 2009

Bias triangle for a suspended DQDs

Bias triangle

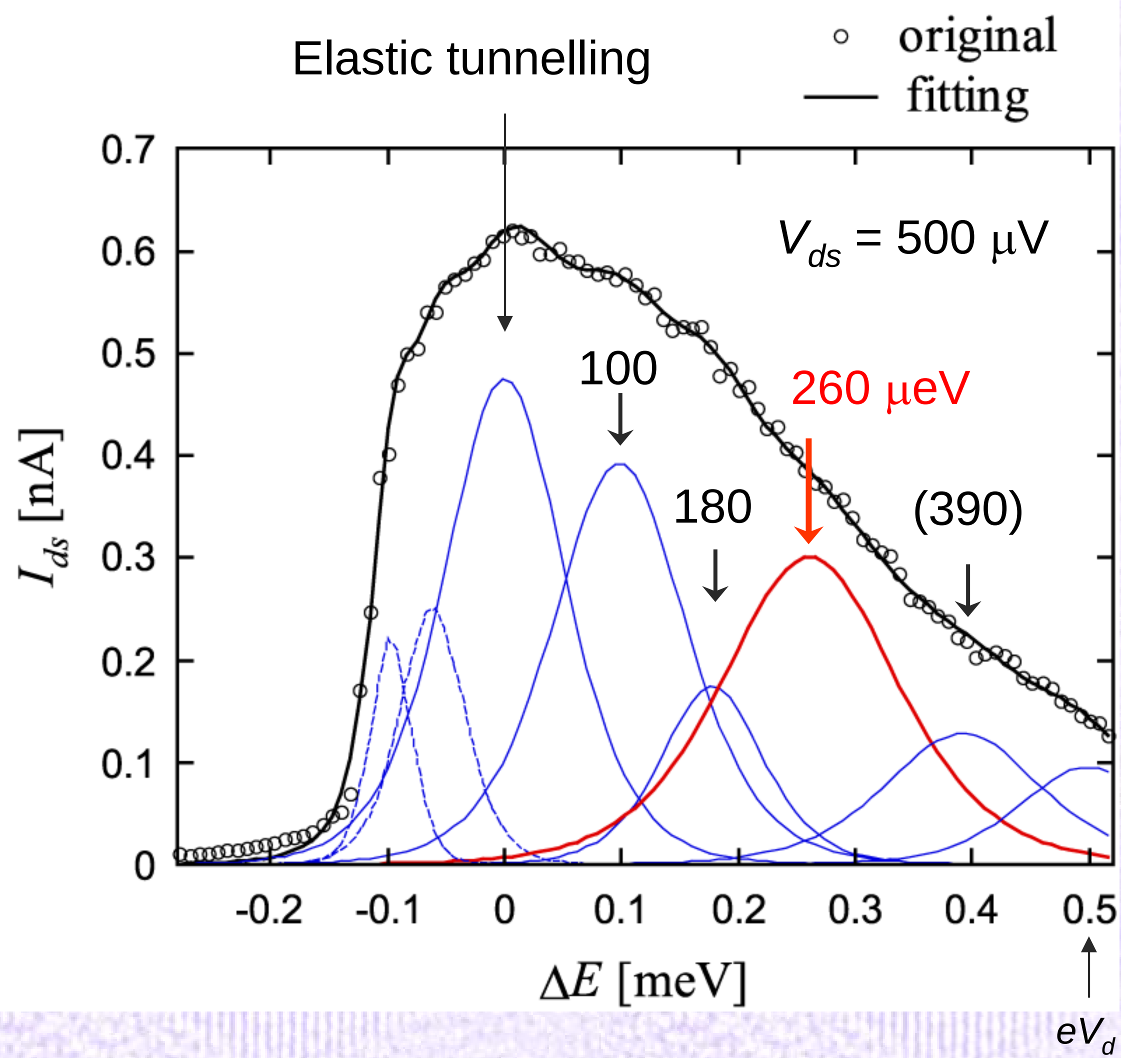


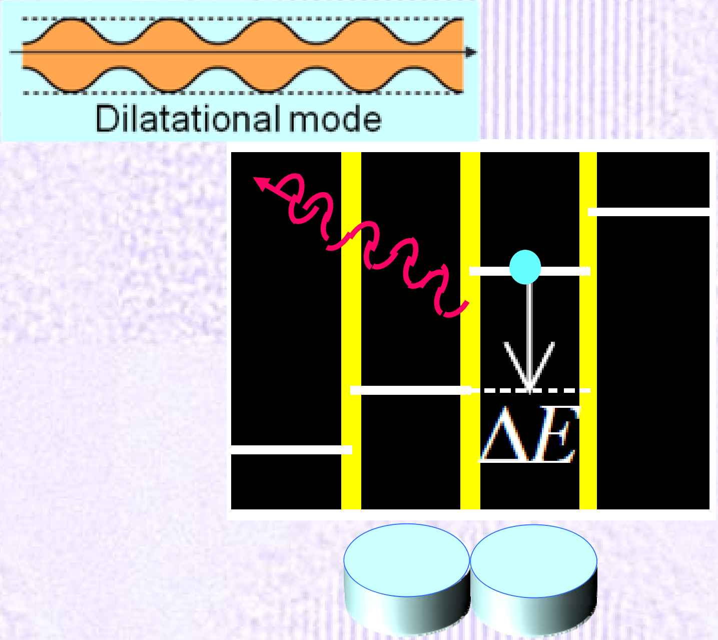


- RT via excited states in QDs
- Phonon assisted tunnelling

J. Ogi, *T. Ferrus, T. Kodera, Y. Tsuchiya, K. Uchida, D. A. Williams, S. Oda and H. Mizuta in press for Jpn. J. Appl. Phys. (2010)*

Inelastic tunnelling via slab phonons



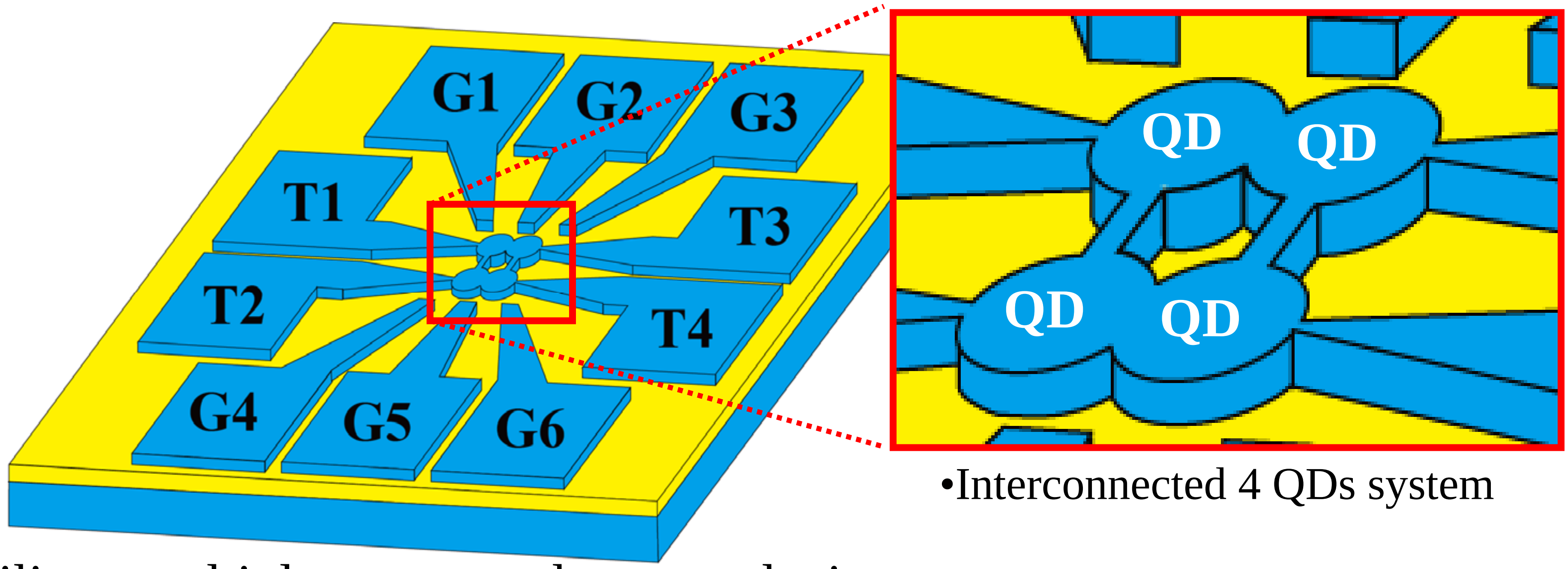


Fundamental processes in which single electrons lose energy in scaled Si NEM structures

J. Ogi, *T. Ferrus, T. Kodera, Y. Tsuchiya, K. Uchida, D. A. Williams, S. Oda and H. Mizuta in press for Jpn. J. Appl. Phys. (2010)*

Electron transport in the Si multiple quantum dots

- Electrostatic and tunnel coupling
- Interplay between the orbit, valley and spin degree of freedom

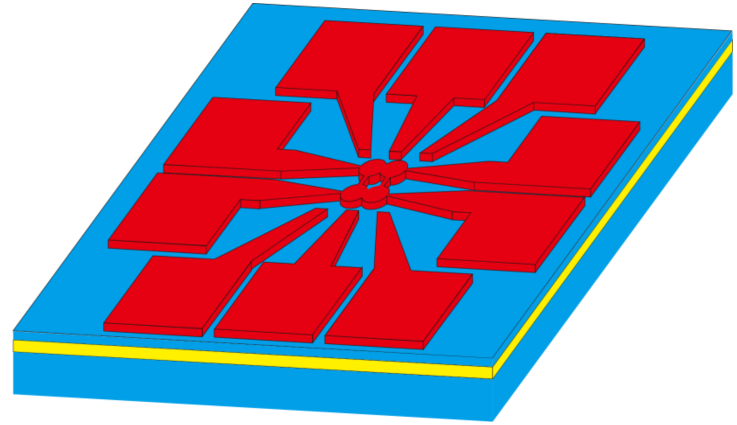


Silicon multiple quantum dot array device

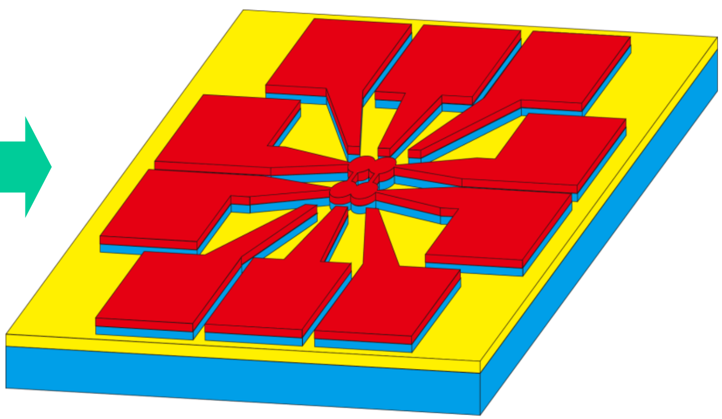
•Interconnected 4 QDs system

Device Fabrication Process

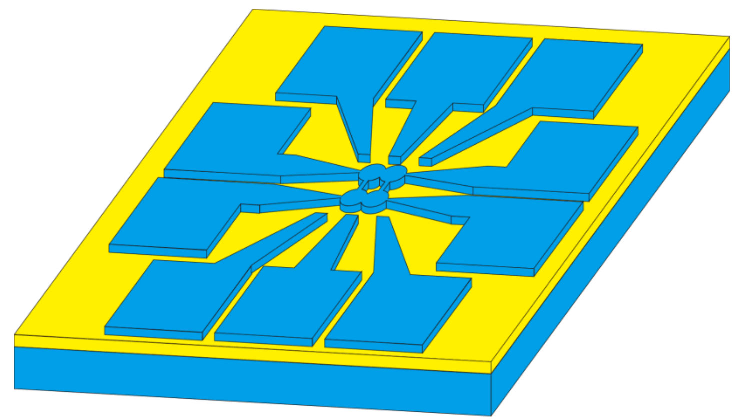
SOI : 40nm、BOX (SiO_2) : 200nm
Doping: P (~1×10^{19} cm^{-3})



EB Lithography

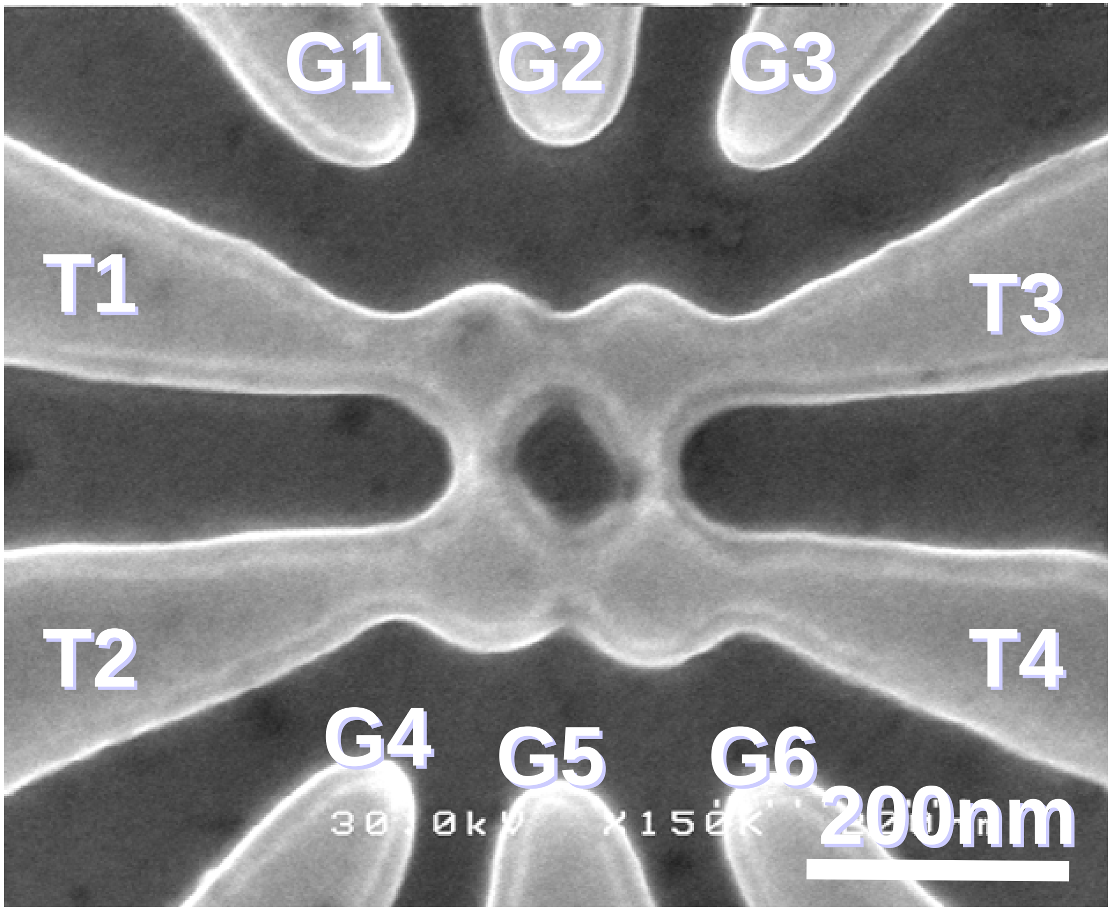


Dry Etching (ECR-RIE)



Thermal Oxidation (1000℃)
（Followed by Al bonding pad）

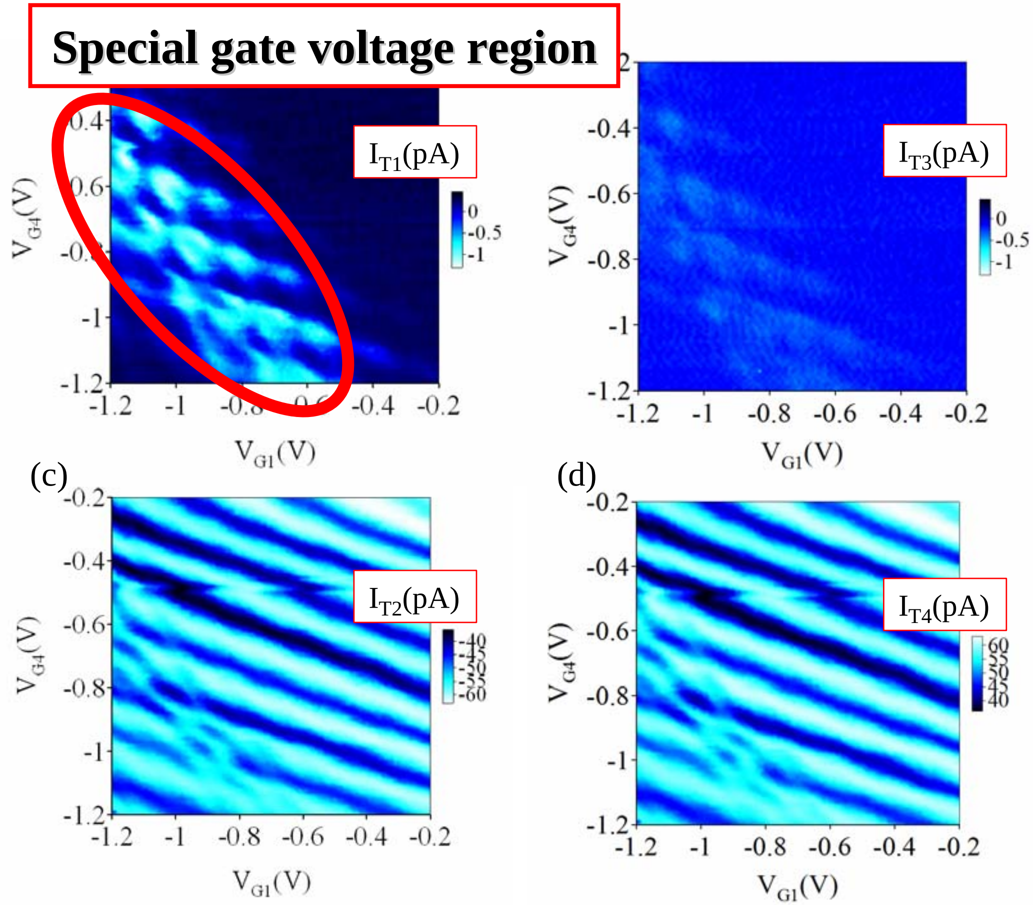
SEM Image of 4 QDs System

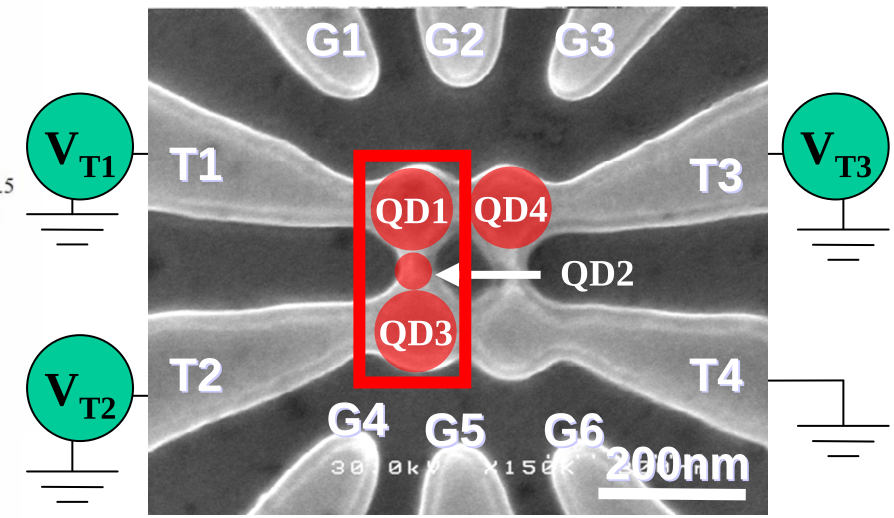


Scanning microscope image of the device

Charge stability diagram

$I_{T1} \sim I_{T4} - (V_{G1}, V_{G4})$ characteristics ($V_{T1} \sim V_{T3}$ = -6 mV, V_{T4} = 0 mV)

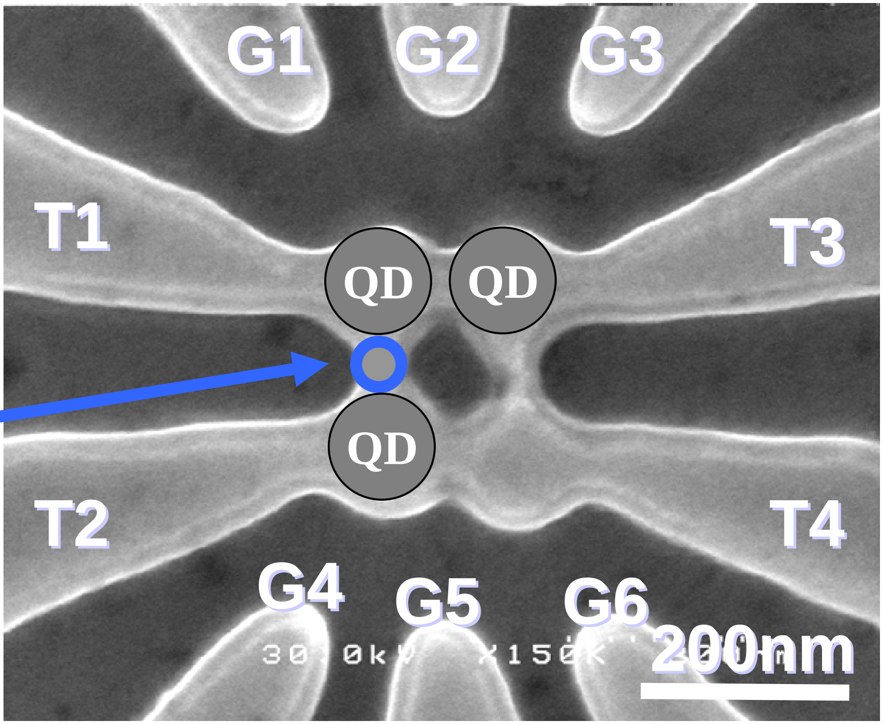




Following discussion supports the validity of actual formed QDs

<u>First observation for electron transport through Si triple quantum dots (TQDs)</u>

Additional small QD

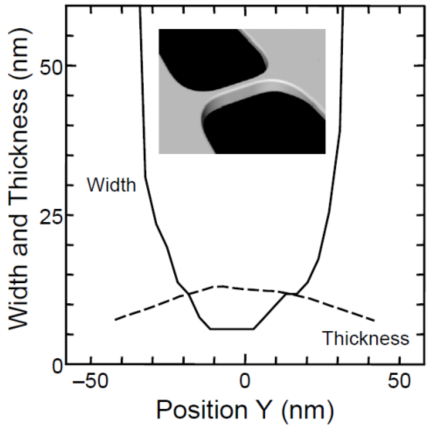


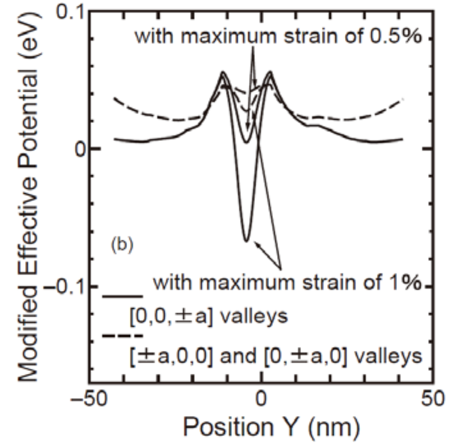
Additional small QD

Mechanism: PADOX (Pattern-Dependent Oxidation)

- Compressive stress due to oxidation
- Quantum-mechanical size effect

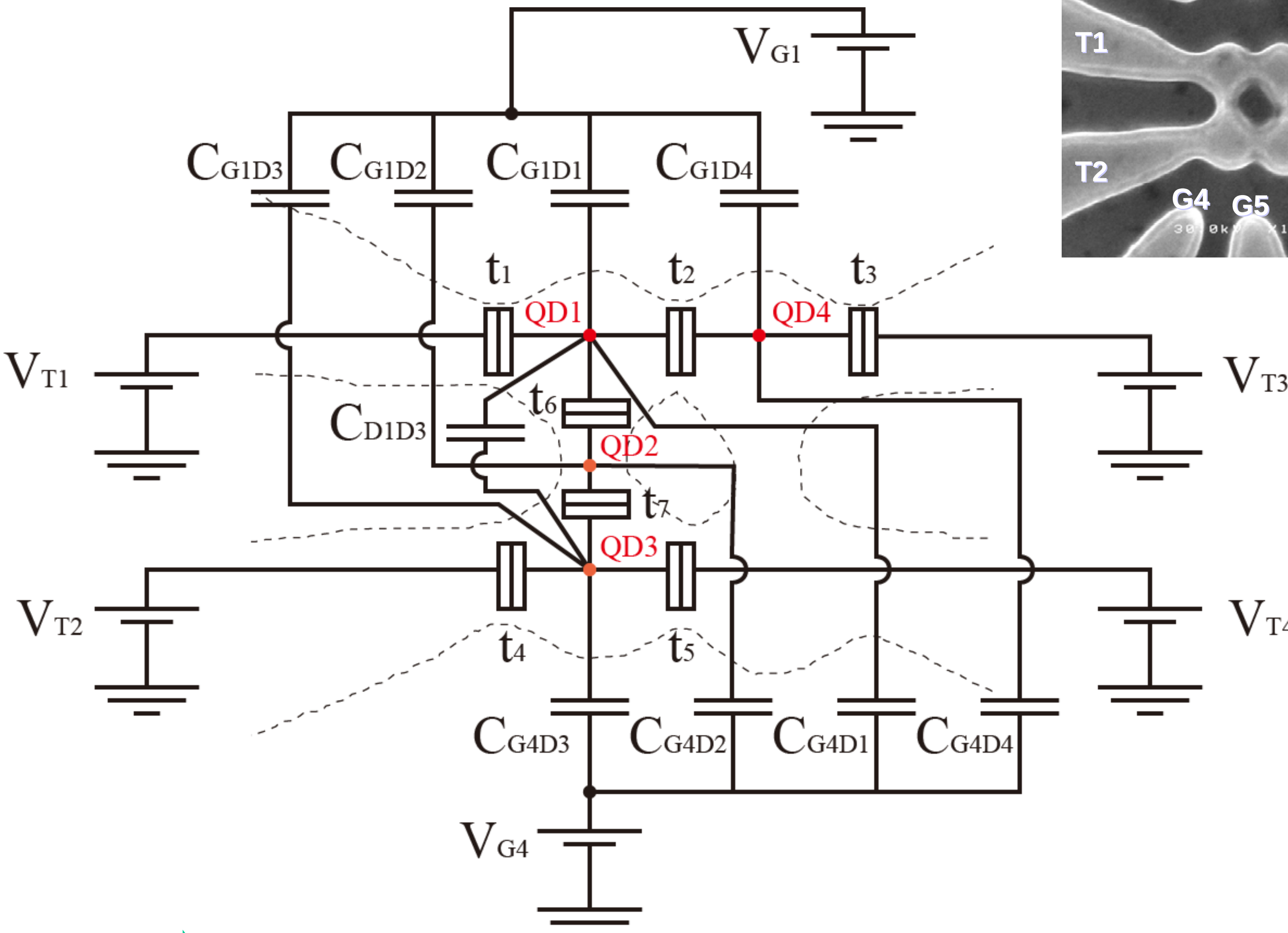
Formation of small QDs

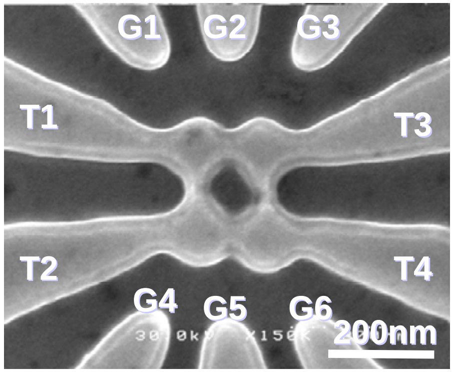




H. Horiguchi *et al*. Jpn. J. Appl. Phys. **40**(1A/B), pp. L29-L32, 2001.

Equivalent circuit model

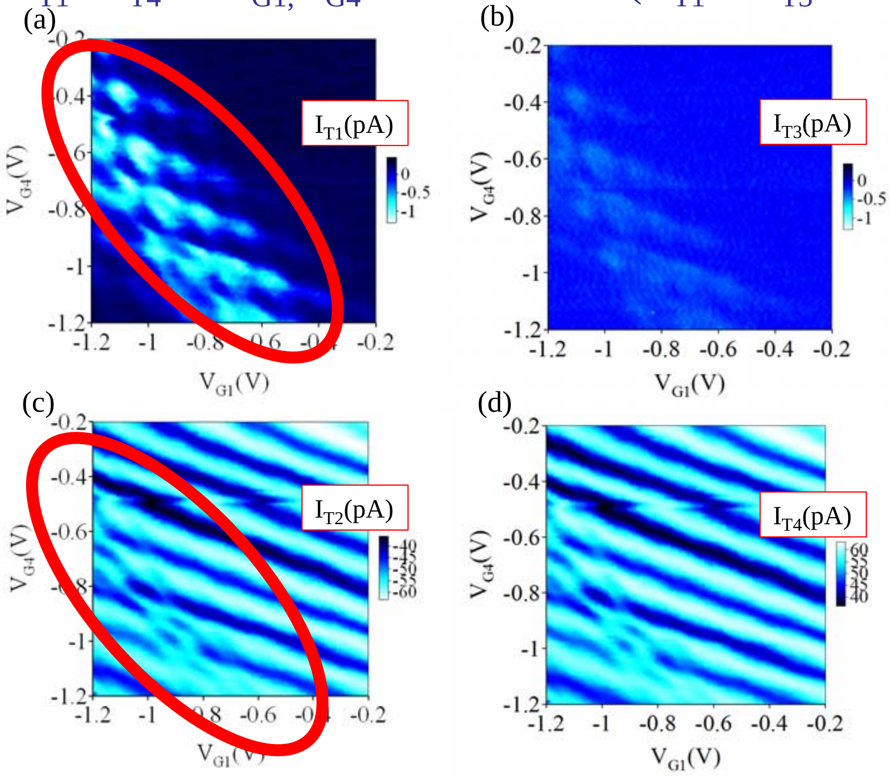


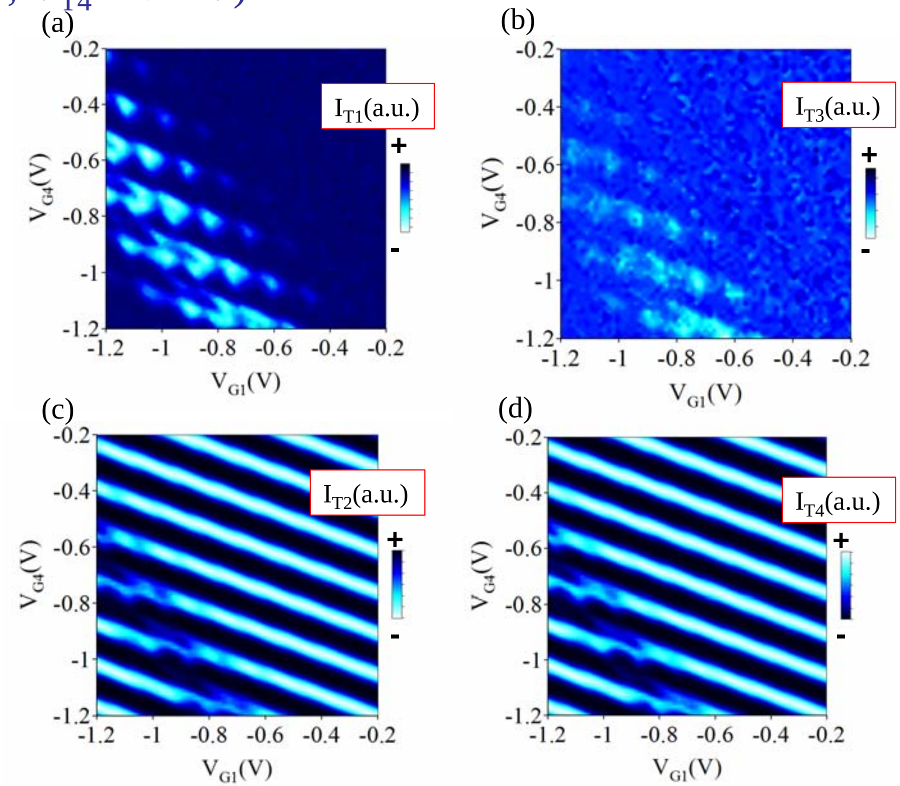


Equivalent circuit simulation

Experiment vs equivalent circuit simulation

$I_{T1} \sim I_{T4}$ vs V_{G1}, V_{G4} characteristics ($V_{T1} \sim V_{T3}$ = -6 mV, V_{T4} = 0 mV)

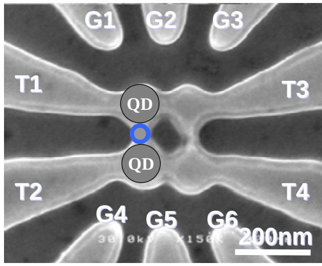




Experimental data

Equivalent circuit simulation

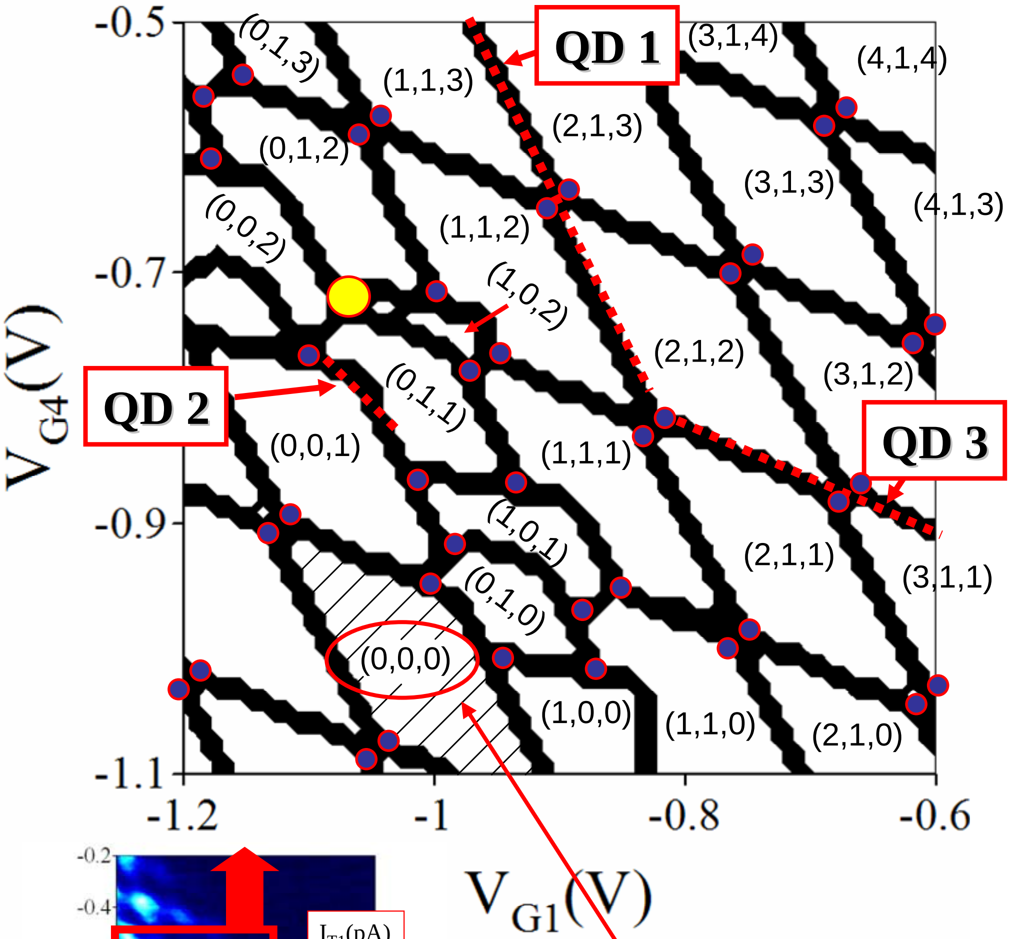
Excellent agreement

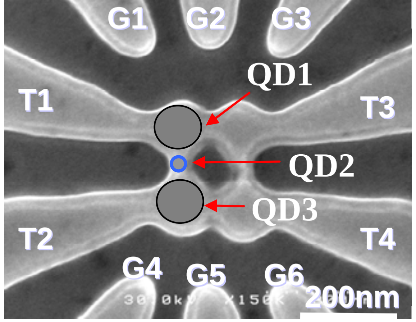


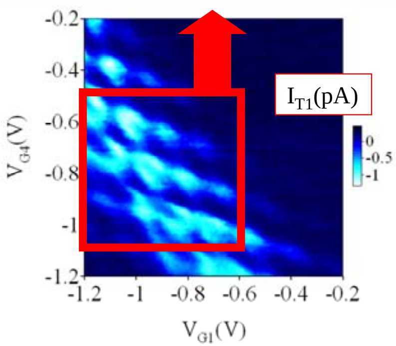
Forms the additional small QD

Electron transport through TQDs

Simulated stable electron numbers in TQDs







Assuming that
the electron numbers are zero
(Not absolute number)

TQDs charge stability diagram

Charging lines:
Electron configuration changes

Two charging lines meet

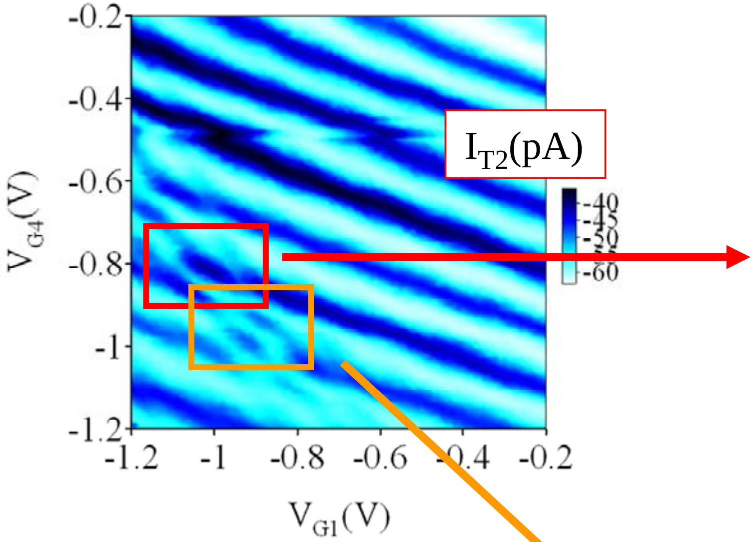
Charge triple points
(2^{nd} order tunneling in TQDs)

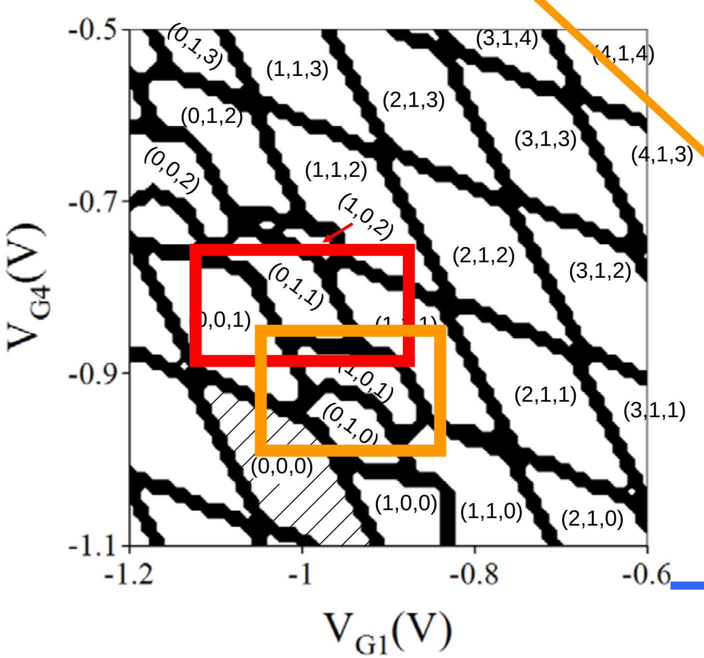
Two charge triple points meet

Charge quadruple points
(Sequential tunneling in TQDs)

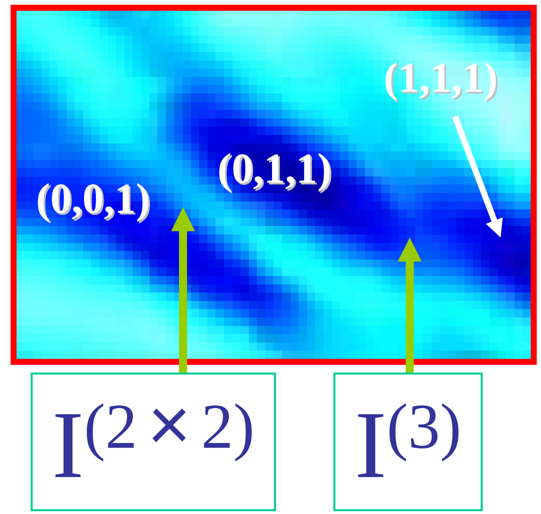
☆Resonant tunneling

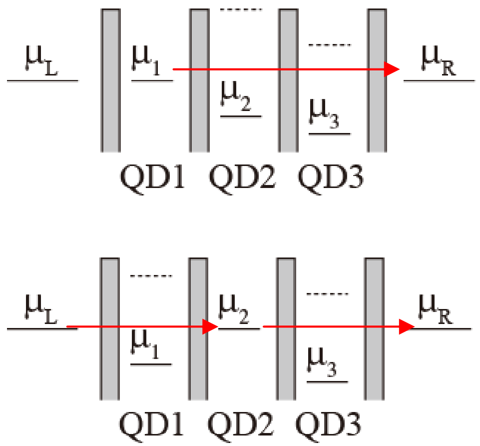
Higher order electron tunneling

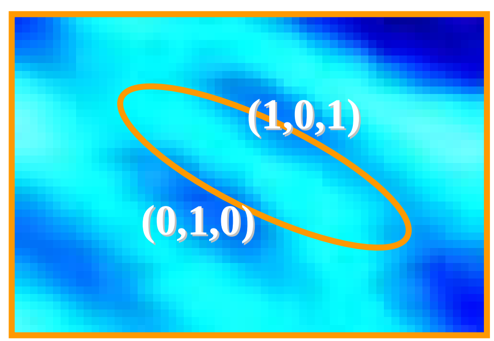




- 3rd order tunneling process $I^{(3)}$
- Two successive 2nd order tunneling $I^{(2\times 2)}$







QCA cotunneling process

(0,1,0) ⇔ (1,0,1)

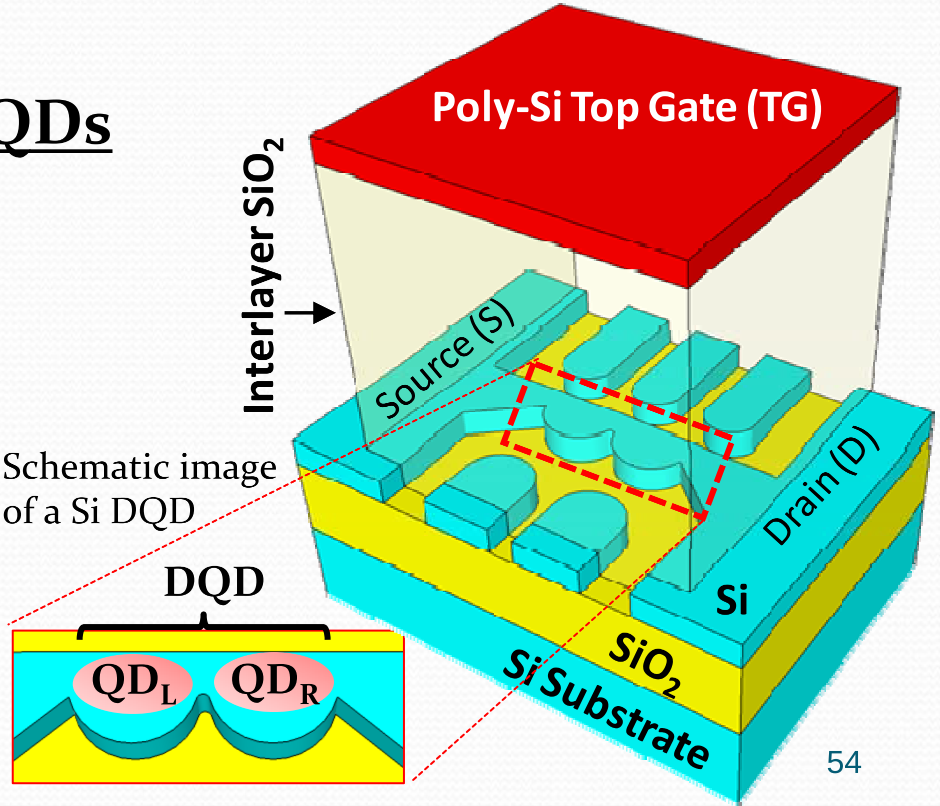
Two electrons move simultaneously
⇒QCA process

D. Schroer *et al*. Phys. Rev. B **76**(7), 075306 (2007).

Investigation of a Pauli spin blocade in controlled pure Si DQDs and its leakage current

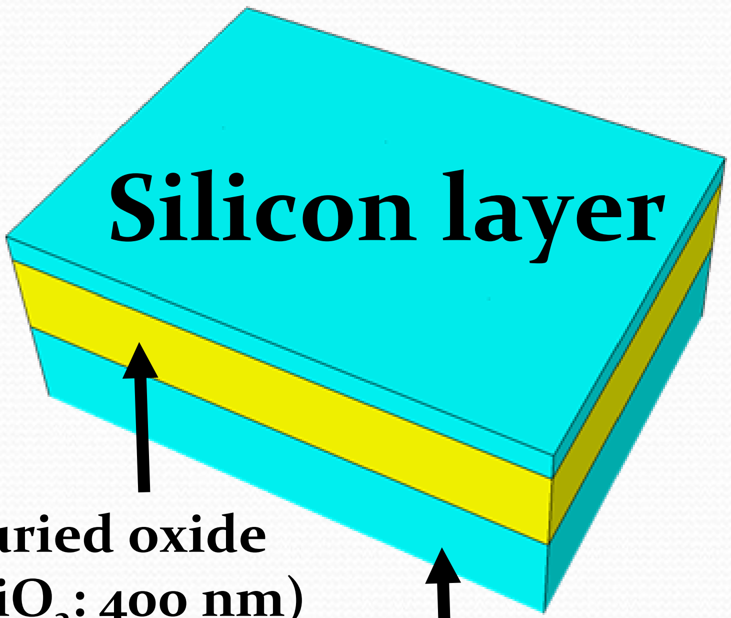
Lithographically-defined Si DQDs

- The DQD is defined by 3 tunnel barriers at 3 constricted regions due to the quantum size effects
- There are five side gates to control the potentials of the DQD and the inter-dot tunnel coupling
- Poly-Si top gate induces carriers in Si layer



G. Yamahata *et al.*: Appl. Phys. Express. **2**, 095002 (2009)

Device Fabrication Process



- **Initial wafer: Si on insulator (~60 nm)**

  Control of the thickness by thermal oxidation
- **Patterning of a DQD and side gates**

  Electron beam lithography followed by reactive ion etching with Cl_2 gas
- **Formation of gate oxides**

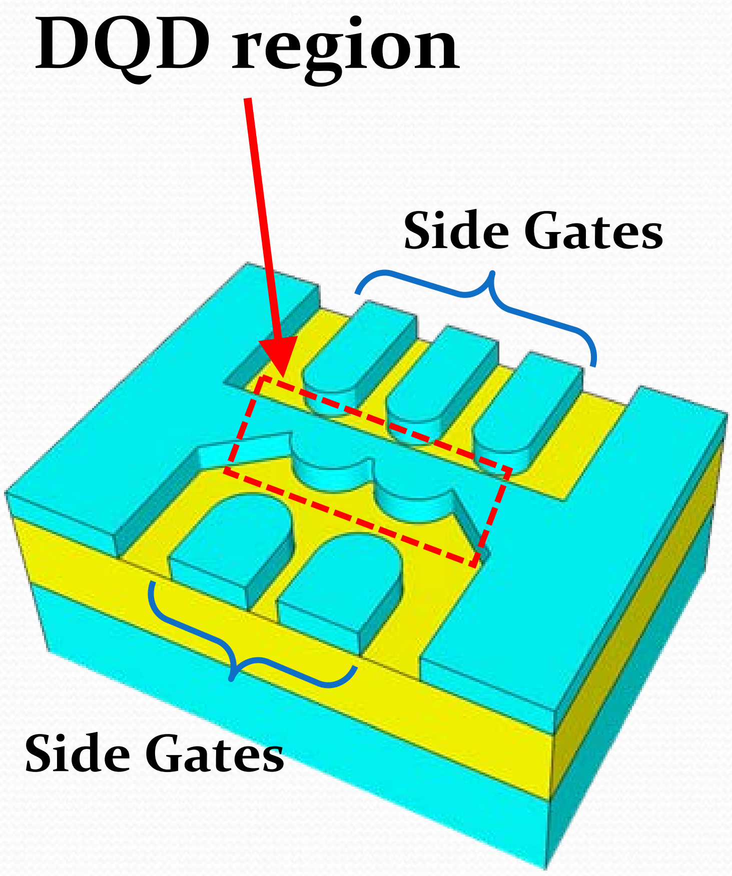
  Thermal oxidation (30 min at 1000 ℃) and LPCVD (thickness: ~35+90 = 125 nm)
- **Formation of poly-Si top gate**

  LPCVD (thickness: ~200 nm、P: ∼10^{20} cm^{-3}) Photo lithography, Plasma etching
- **Formation of source (S) and drain (D)**

  Ion implantation (P: ∼10^{19} cm^{-3})

  Bonding pads(Al) fabricated by Photo lithography and EB evaporator

Device Fabrication Process



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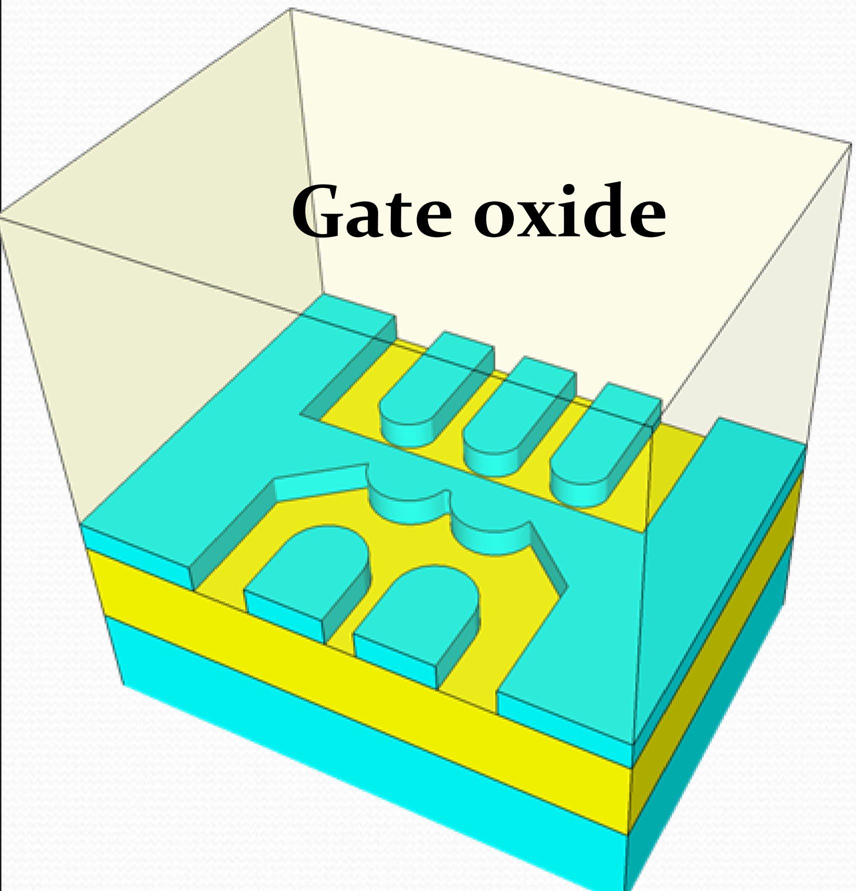

(Actual thickness of the gate oxide is thinner than that in the schematic image.)

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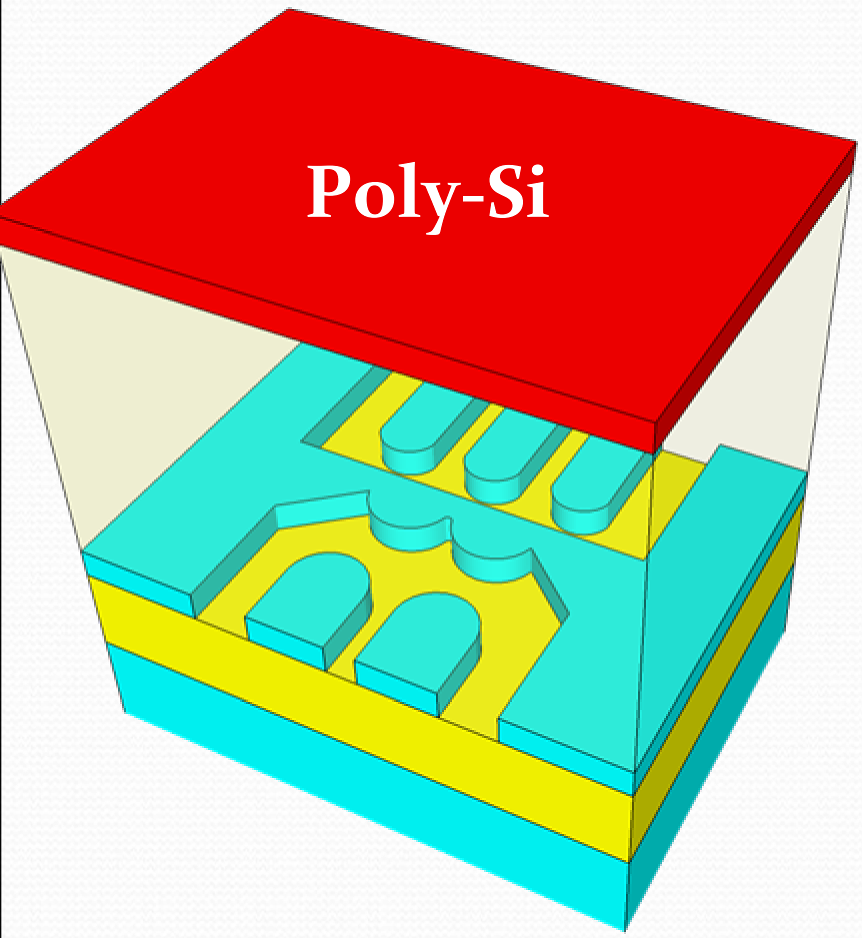

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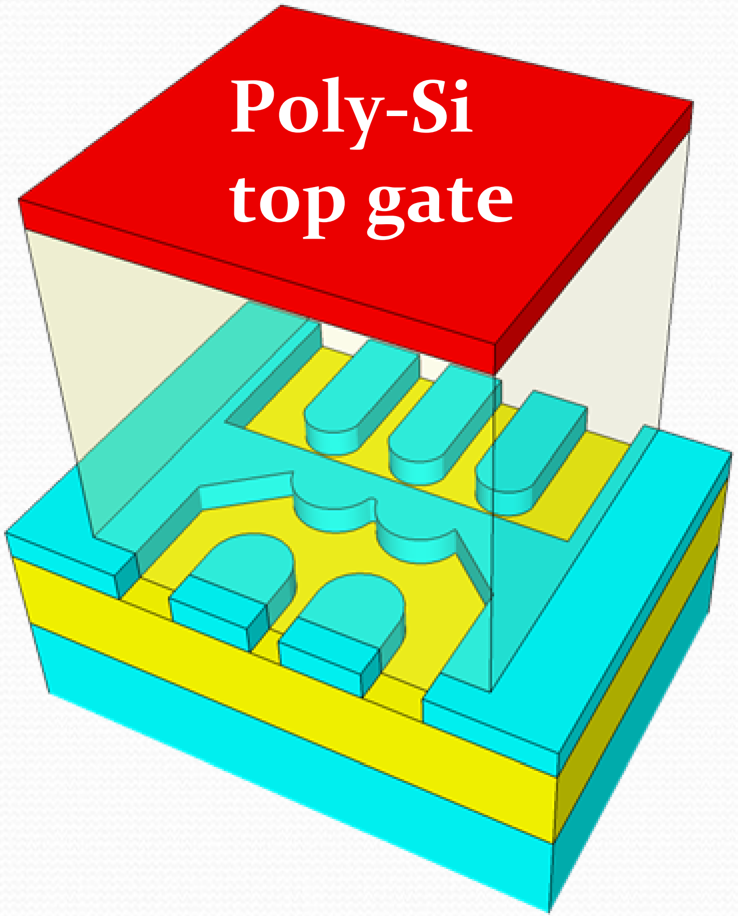

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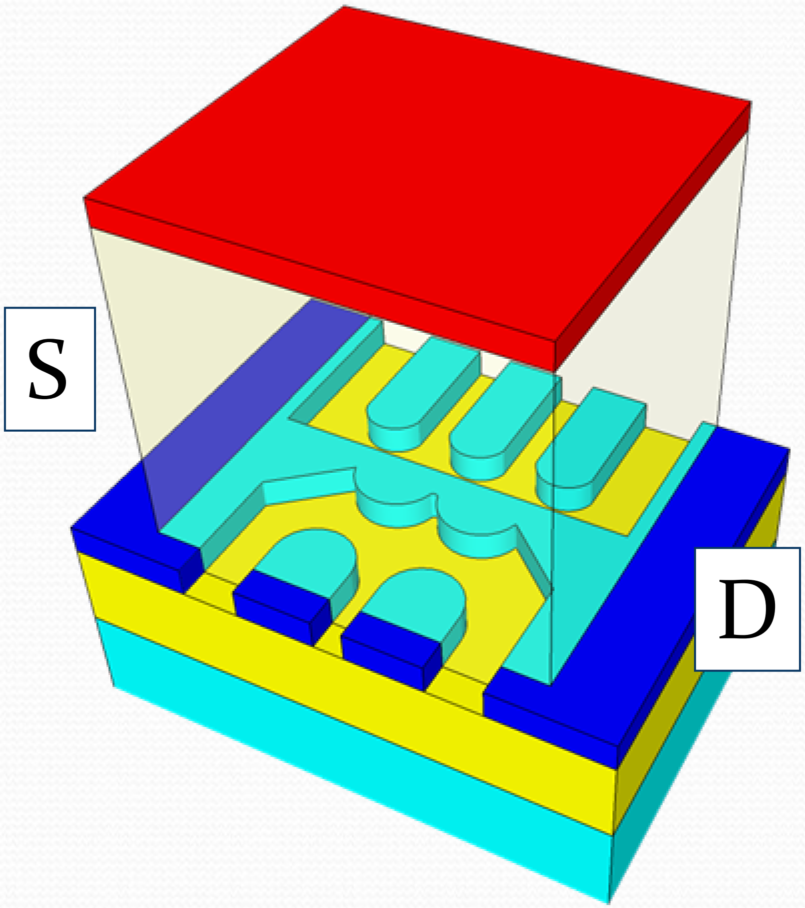

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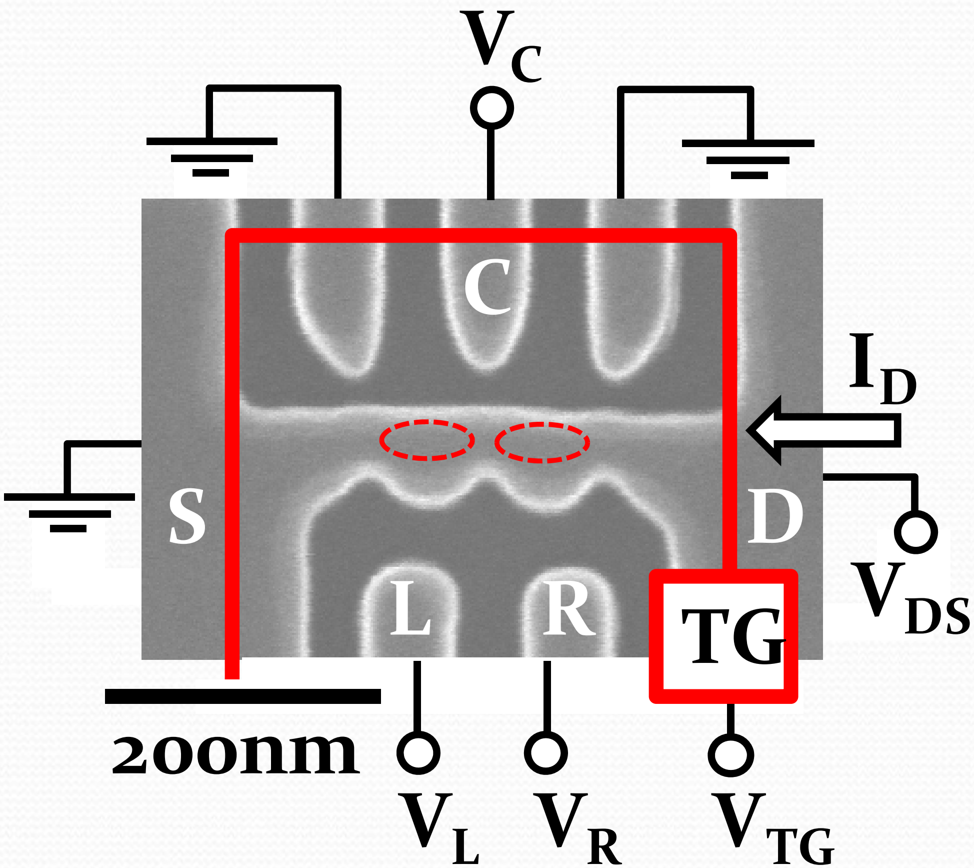
Fabrication results



SEM image of the Si DQD

Top gate (TG)
Induce carriers to the Si DQD with constant positive voltages

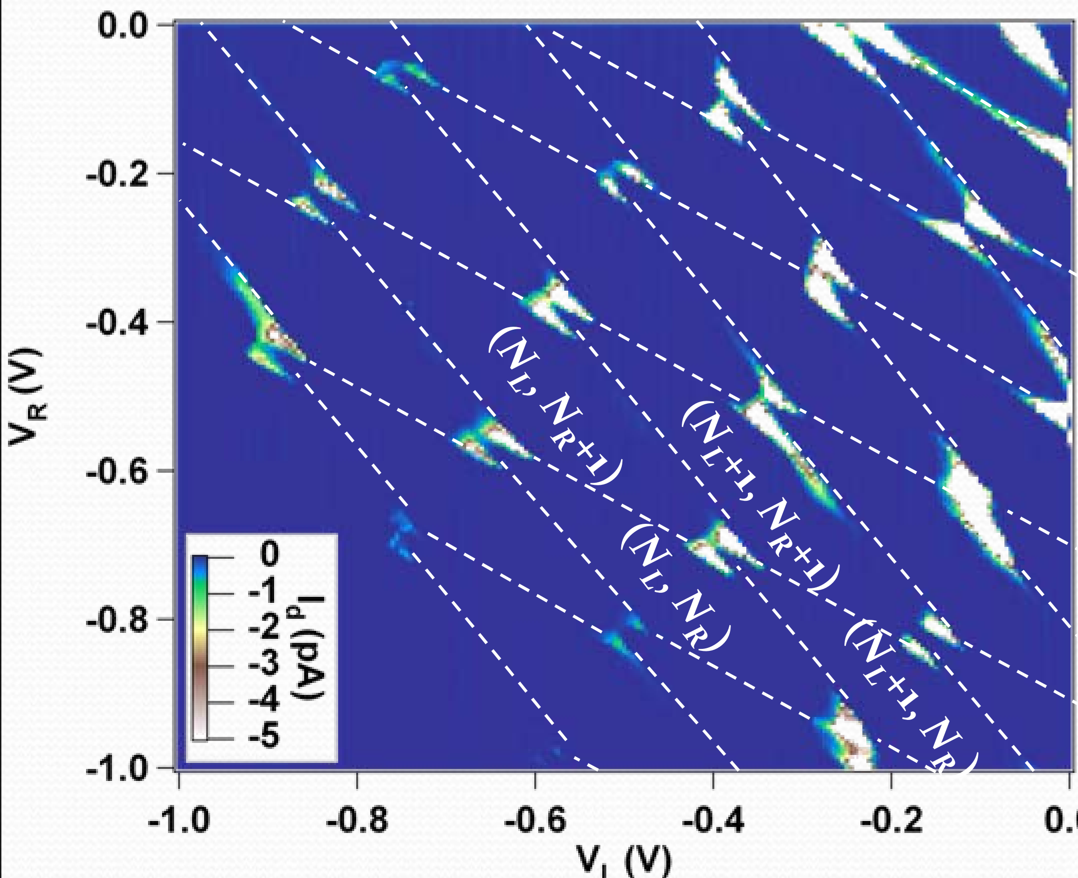
Side gates L & R
Modulate the electrochemical potentials of the left & right QDs

Side gate C
Tune the tunnel coupling between left & right QDs

Measurement setup (Marcus group in Harvard University)

- ^{3}He refrigerator with a base temperature of 250 mK
- DC measurements with voltage sources, DACs, current preamplifiers, and digital multi-meters

Charge stability diagram



Charge stability diagram of the Si DQD
(V_{ds} = -2 mV, V_{TG} = 900 mV, and V_C = -1.72 V)

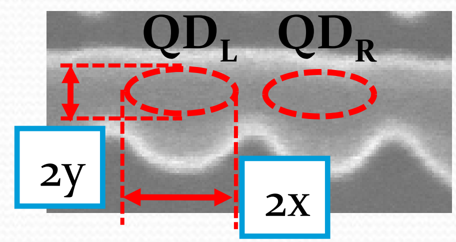
Honeycomb diagram of a Si DQD coupled in series

	Charging energy E_C	Quantum level spacing ΔE
QD_L	10.7 (meV)	310 (μeV)
QD_R	11.0 (meV)	260 (μeV)

(ΔE was estimated from resonant tunnel peaks of one of triple points)

$$\Delta E = \frac{\hbar^2}{2m^* xy}$$

(m*: effective mass)

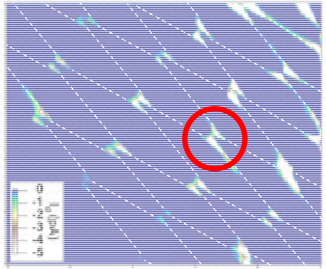


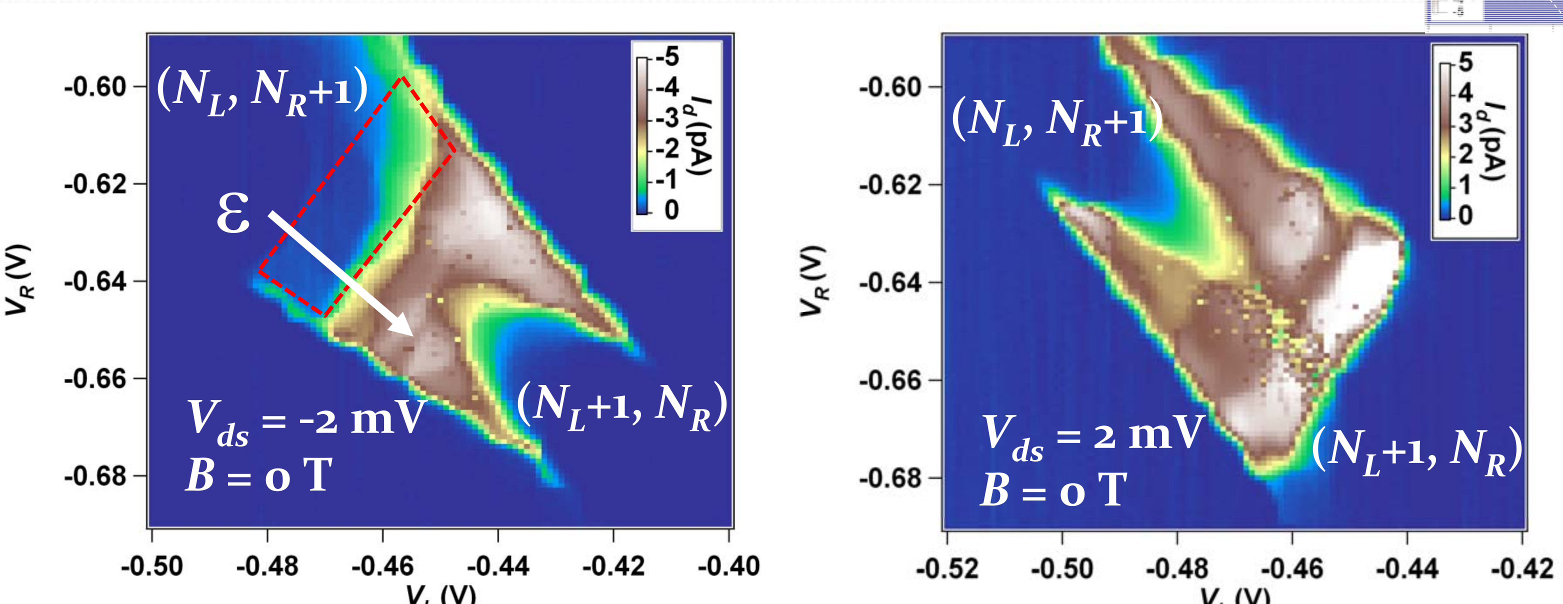
⇒ 250 ~380 μeV (10 nm size differences)

QD is formed between the two constrictions

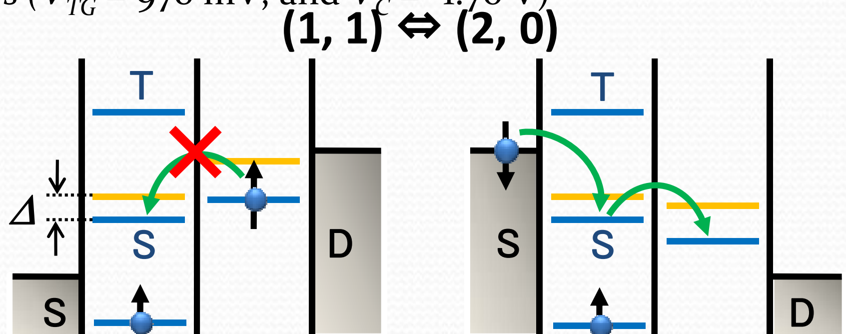
Mesoscopic Electron Transport; L. Sohn *et al.* (1997)

Pauli spin blockade (PSB)





One of triple points of the Si DQDs (V_{TG} = 970 mV, and V_C = -1.76 V)



Current rectification only at negative bias

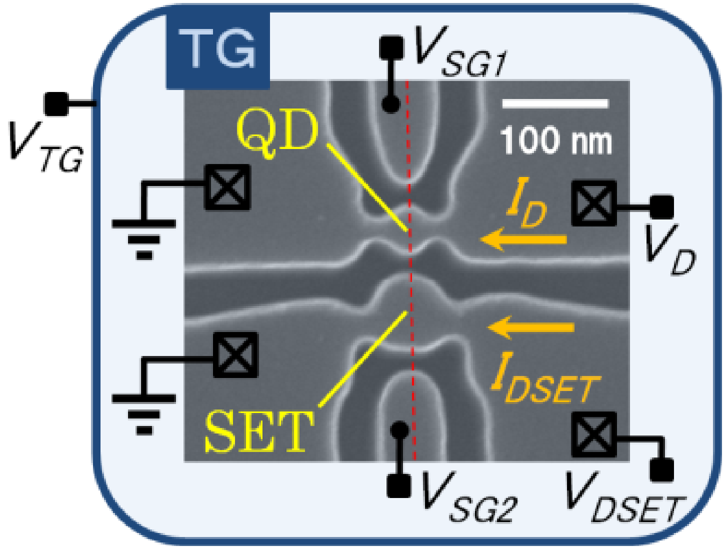
➡ **PSB in the controlled Si DQD**

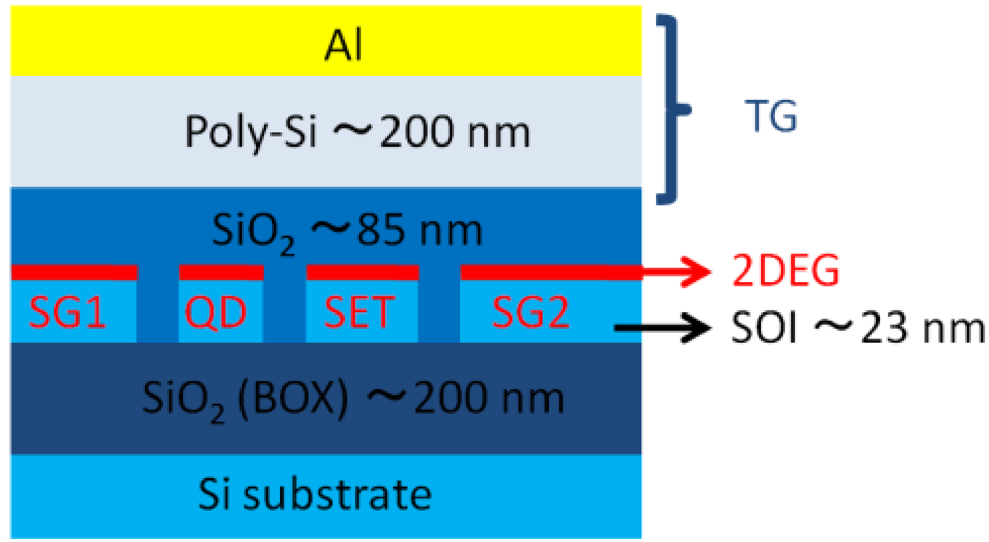
Although Si has multivalley, a theory have shown that the PSB occurs

D. Culcer *et al.* arXiv:1001.5040 (2010)

Schematic energy diagrams including two valleys

Integration of QD and charge sensor SET



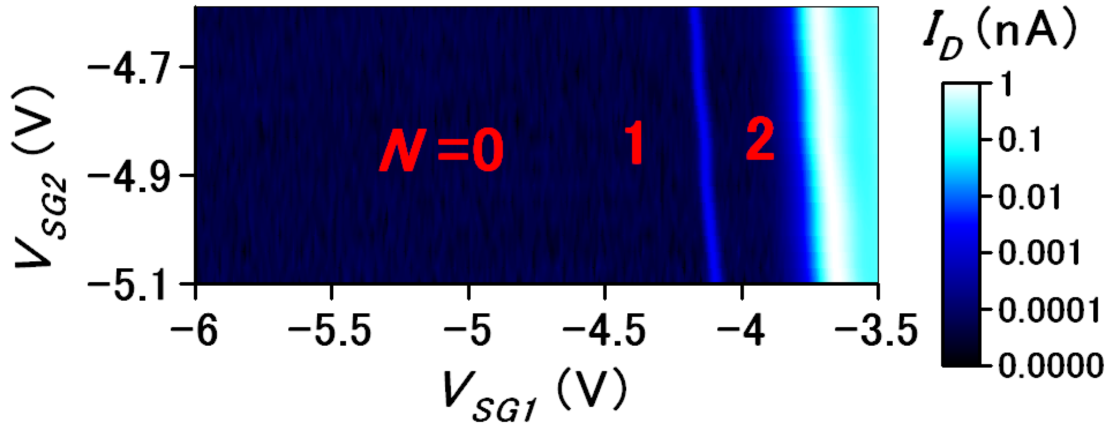


- SET charge sensor is useful for detection of a few electrons in quantum dots.

Observation of a single electron state

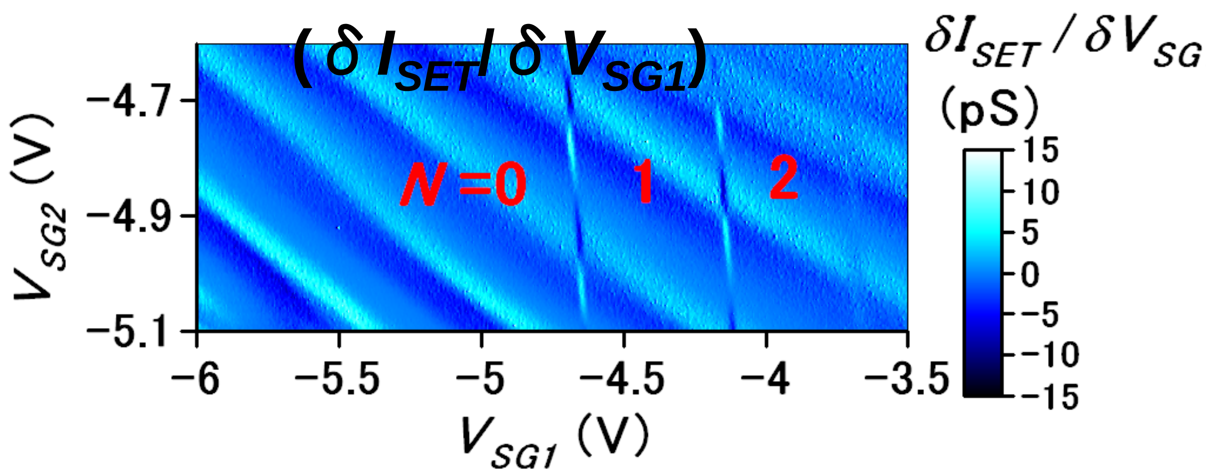
4.2 K

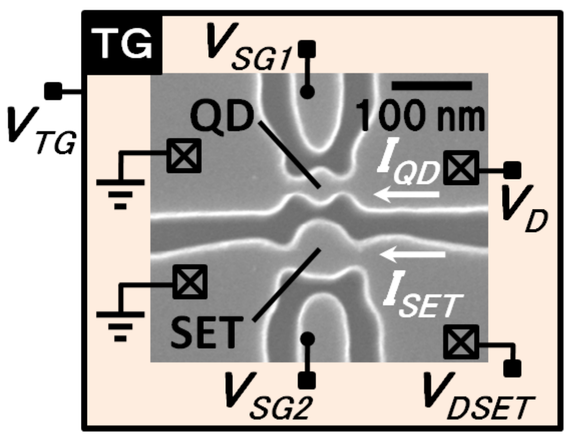
➢**QD current (I_D)**



P-2
P-5
P-9
P-10
P-11
P-12

➢**SET conductance ($\delta I_{SET}/\delta V_{SG1}$)**





V_D=1 mV, V_{TG}=3.8 V, V_{DSET}=5mV

K. Horibe (EP2DS 2011)

Conclusion

- **Integrated NeoSilicon**

  high-on/off transistors, photovoltaic

- **NEMS Memory**

  ultralow-power, very long retention time

- **Nano-bridge Transistors**

  nano-phonon, emerging research field

- **Coupled Quantum Dots**

  Pauli spin blockade